Setup and Operations with the DBBC3

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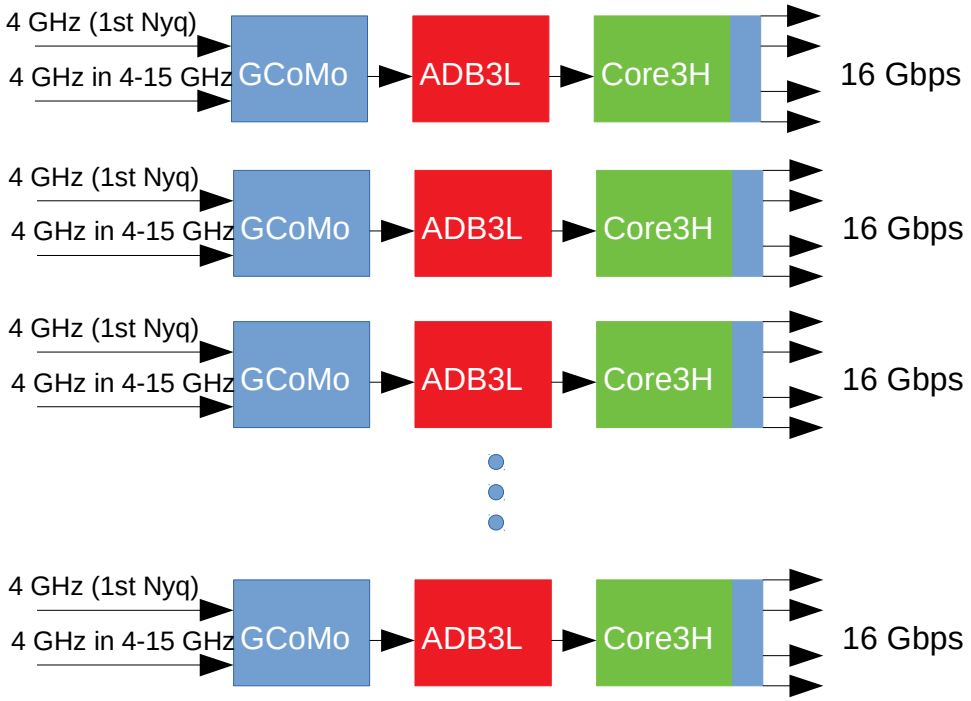
Contents

Introduction

- Digital Baseband Converter for VLBI Observations
- Successor of DBBC2
- 2-8 IF with 4 GHz input bandwidth
- Optional downconversion that converts a 4 GHz band within the range of 4-15 GHz downto 0-4 GHz for each IF
- Provides multiple observation modes for geodetic and astronomic observations
- Output VDIF over up to four 10GBit/s SFP+ connectors for each IF, up to 128 Gbit/s maximum output datarate for 8 IFs.

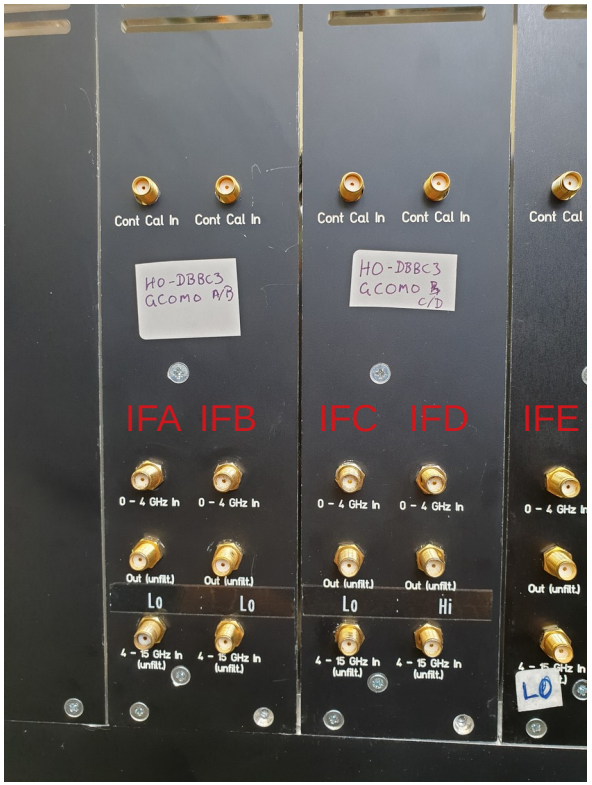
Structure



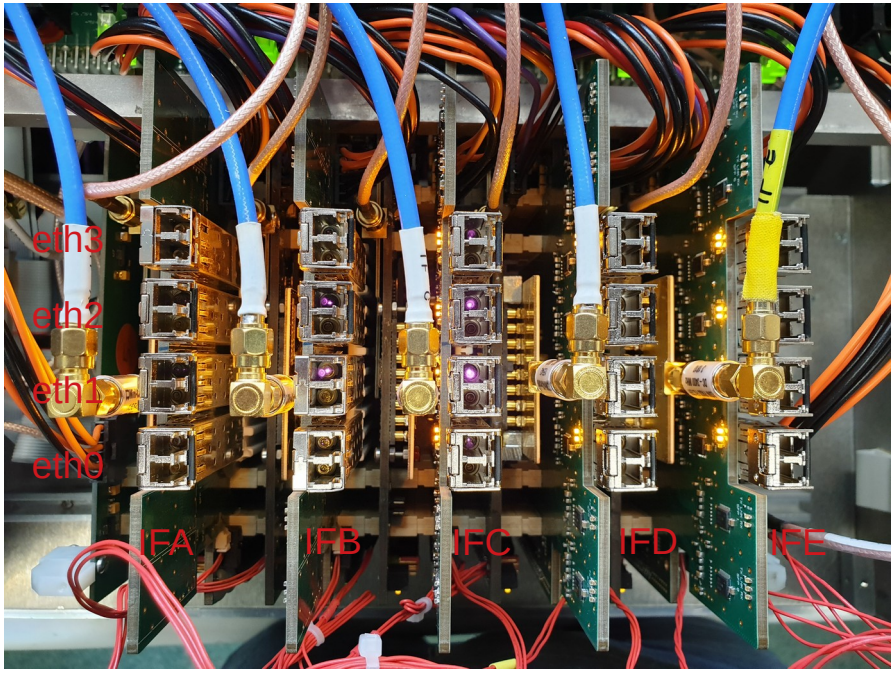
- GCoMo: Analog signal processing
  automatic gain control
  power level monitoring
  optional downconversion (4-15 GHz → 0-4 GHz)
- ADB3L: Analog Digital Converter
  4-way interleaved sampling @ 2048 MHz
  → 4096 MHz bandwidth
  output: 8Gsps @ 10 Bit
- Core3H: Digital Postprocessing
  digital filtering, depending on observation mode
  time and 1PPS synchronization
  monitoring of sampler statistics
  creation of VDIF packets and data transmission to recorders (up to 16 Gbps/IF)

Structure

Analog Inputs:



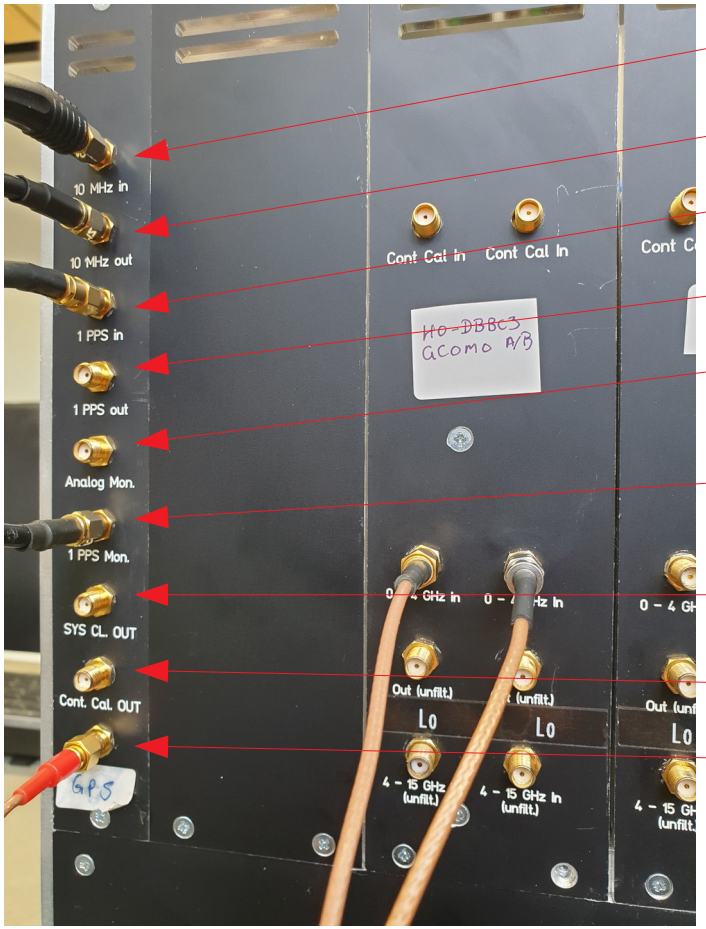
10GE Outputs:



Structure, Components and Connections

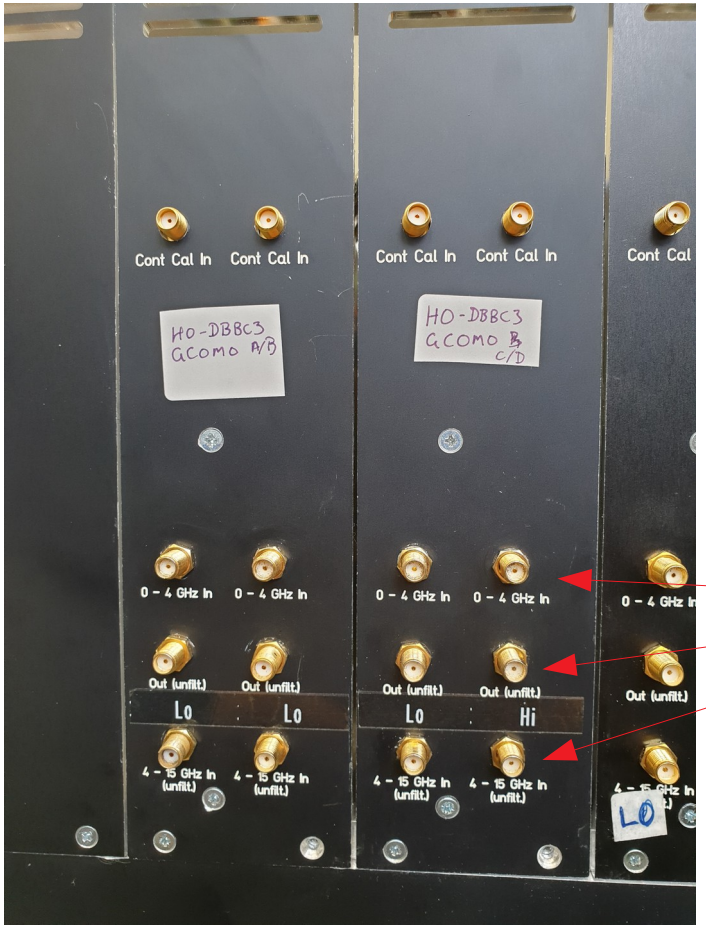
- General Connections (10 MHz, 1PPS, ...)
- GCoMo (Gigahertz Conditioning Module)
- GCAT (Clock Synthesizer and Distribution)
- ADB3L (Analog Digital Converter)
- Core3H (Digital Postprocessing)
- PC Part
- Cooling

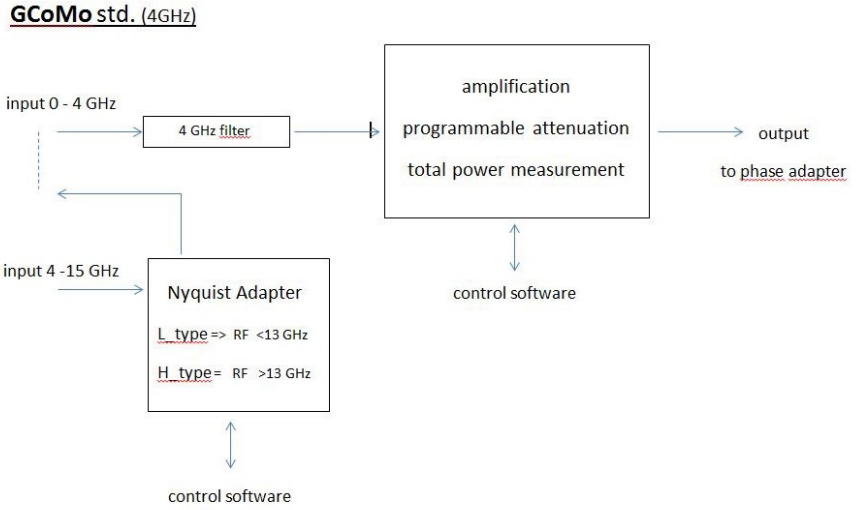
General Connections



- 10 MHz input, from Maser, 0-3 dBm
- 10 MHz output, passthrough from 10 MHz input
- 1 PPS input, from Maser, 5V TTL at 50 Ohm
- 1 PPS output, passthrough from 1 PPS input
- Analog Monitor, connected to DAC with 256 MHz BW, from last Core3H in the Stack
- 1 PPS Monitor, connected to internal 1PPS from last Core3H, used for delay-measurement
- System Clock Output, 2048 MHz system clock
- Cont. Cal Output
- GPS input

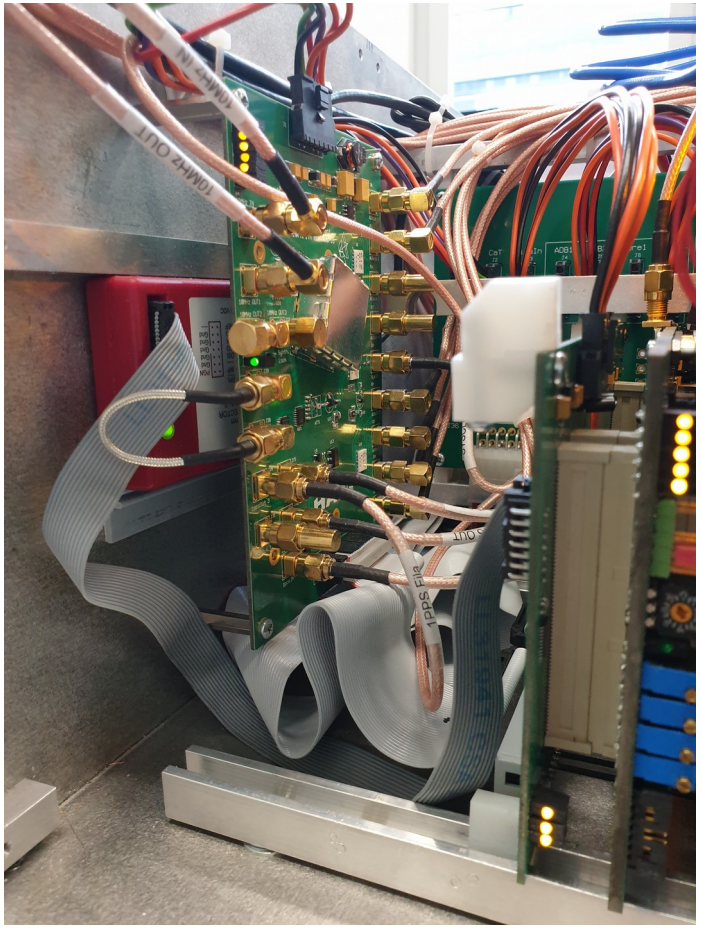
GCoMo – Gigahertz Conditioning Module

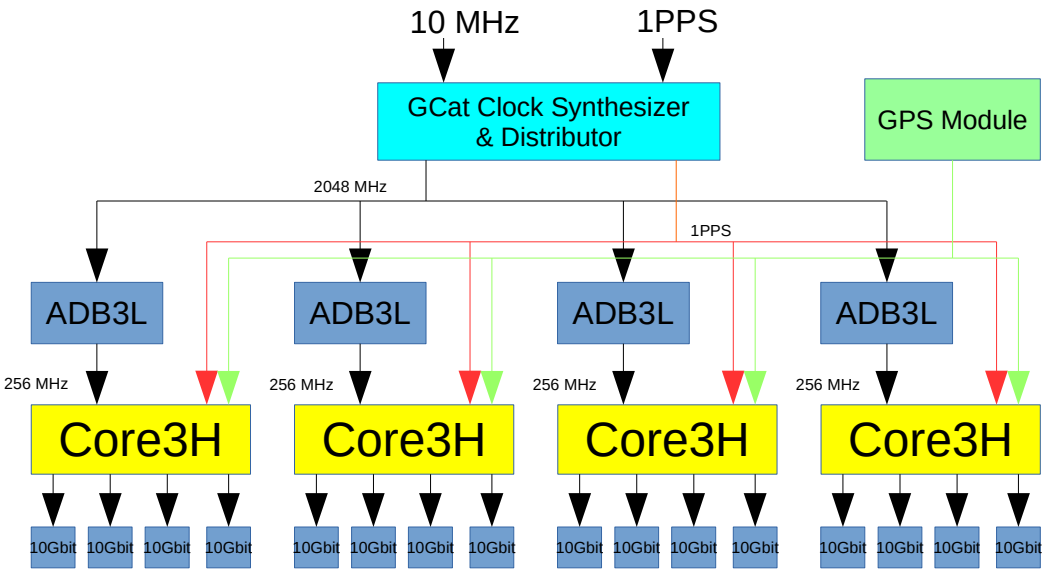




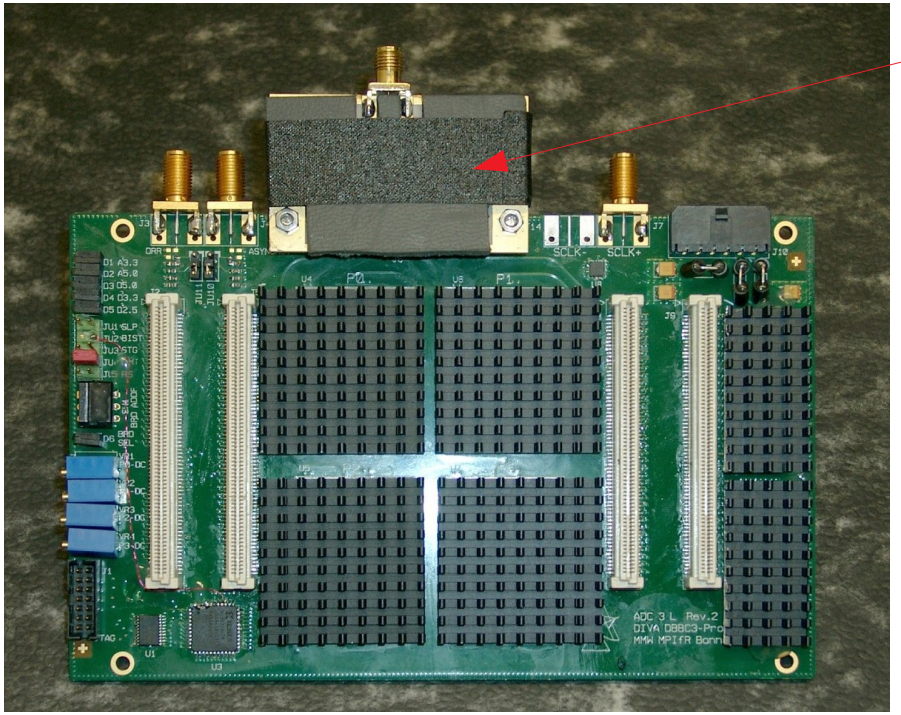
- Input 0-4 GHz, direct or after downconversion
- Output of downconverter, range 0-4 GHz
- Input Downconversion, 4 GHz band in the range of 4-15 GHz.
- Two types of Downconversion:
  L-Type RF < 13 GHz
  H-Type RF > 13 GHz

GCat – Clock Synthesizer and Distribution



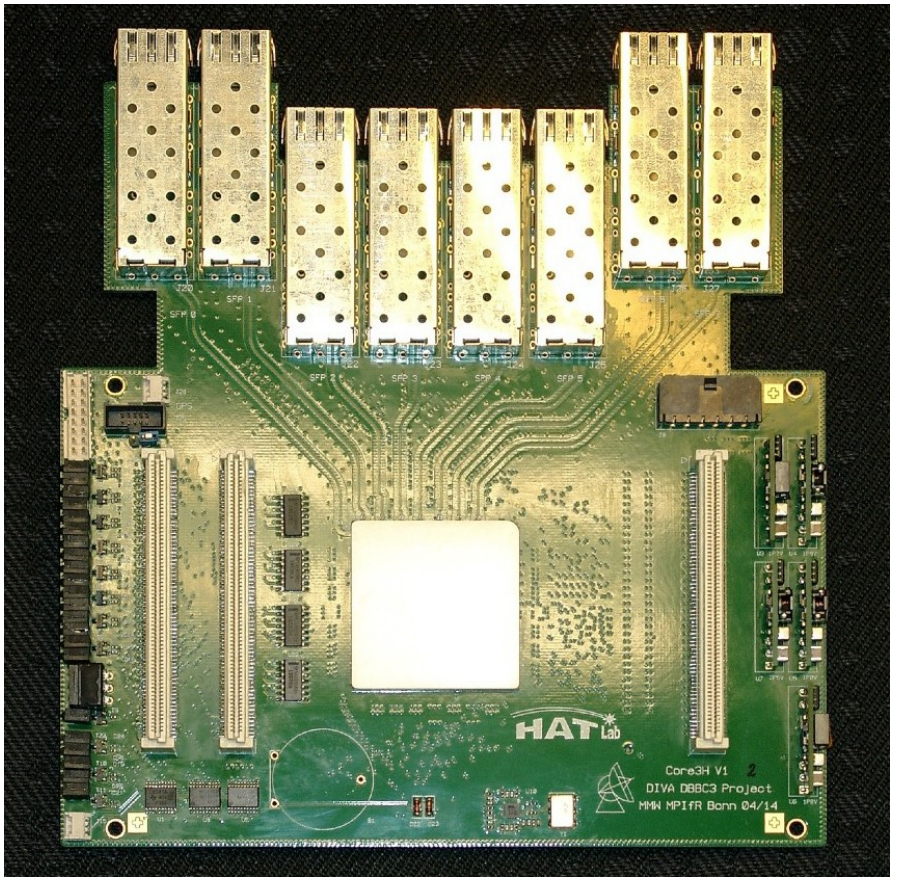


ADB3L – Analog Digital Converter



- Sampling method: 4-way interleaved sampling using four ADC devices each running at 2048 MHz
- Phase Adapter required to distribute the analog signal to all four samplers
- Requires careful calibration of each samplers offset, gain and phase delay to prevent artifacts in the reinterleaved datastream.
- Possible Input Bandwidths: 1x4 GHz, 2x2 GHz, 4x1 GHz
- Output Bandwidth: 8 Gsps @ 10 Bit → 80 GBit/s

Core3H – Digital Postprocessing

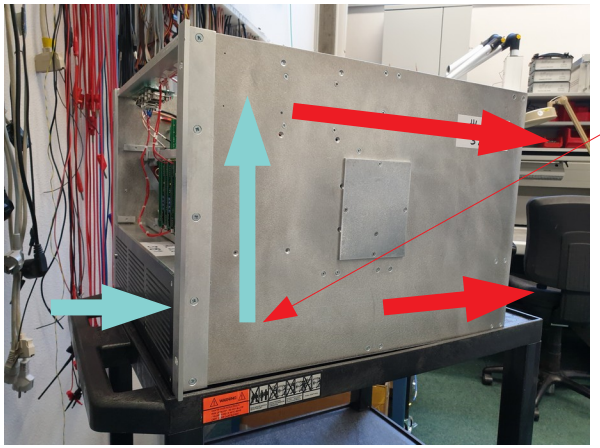


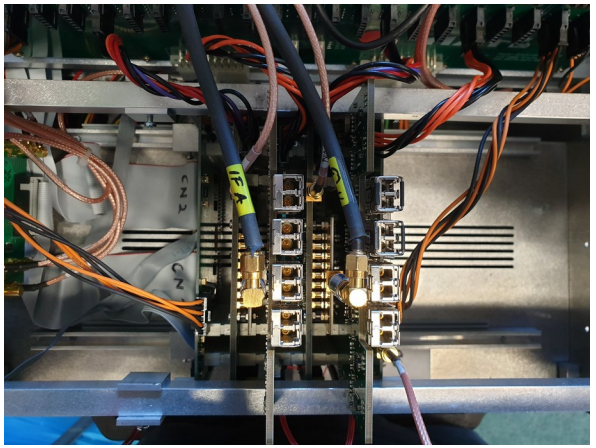
- Digital Postprocessing Board based on Xilinx Virtex 7 FPGA
- Can be controlled with the PC using Serial and PCI-Bus Communication
- Connected to GPS Controller for time synchronization
- Firmware for different observation modes can be loaded using JTAG chain
- Up to eight SFP+ connectors available, four used in existing DBBC3s with maximum datarate of 16 GBit/s

Integrated PC

- Integrated PC running Windows XP for communication with GcoMo/ADB3L/Core3H
- Provides remote control of system via Ethernet connection
- Runs control software that controls/monitors the components using Serial and PCI-Bus communication
- VGA-Port
- Ethernet Connection
- USB Connections
- PS/2 for Mouse/Keyboard

Cooling





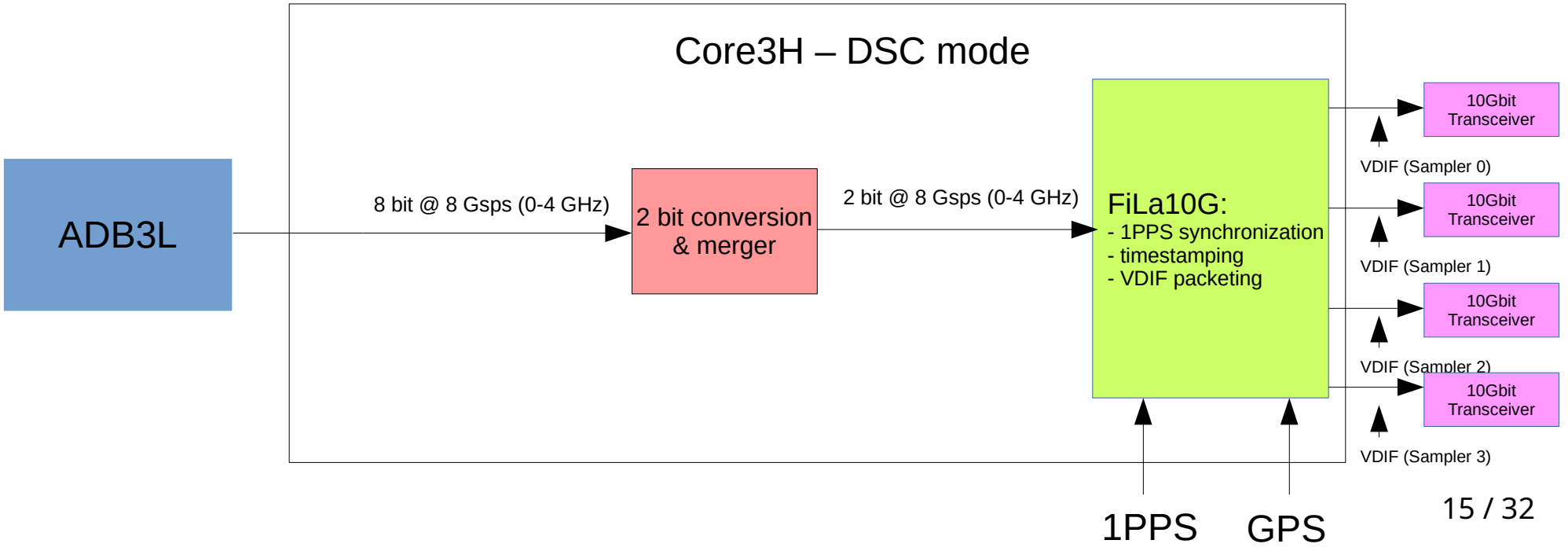
- Airflow, provided by revolver fan in front bottom of the DBBC3
- The stack of ADB3L/Core3H should always be positioned so that the heatsinks are in the airstream
- For a full stack of 8 IFs there is less than a cm tolerance, position of stack needs to be checked after transport!
- Recommended room temperature is 21°C at sea level around the DBBC3, at higher altitude additional cooling might be necessary due to lower air pressure.

Observation Modes

- DSC (Direct Sampling Conversion) full 4GHz Bandwidth/IF
- OCT (Octopus), provides single (OCT_S) or double (OCT_D) 32-tap FIR-Filter/IF
  Available Bandpass-Filters:
  512 MHz BW: 0-512, 512-1024, ..., 3584-4096
  1024 MHz BW: 0-1024, 1024-2048, ..., 3072-4096
  2048 MHz BW: 0-2048, 2048-4096
- DDC (Digital Tunable Downconversion): provides up to 16 BBCs/IF with fully tunable frequency, selectable BW of 1, 2, 4, ..., 128 MHz, depending on the DDC Mode used
- Each observation mode has its own control software/firmware/ set of configuration files.
- Newest versions can be downloaded at https://www.hat-lab.cloud/

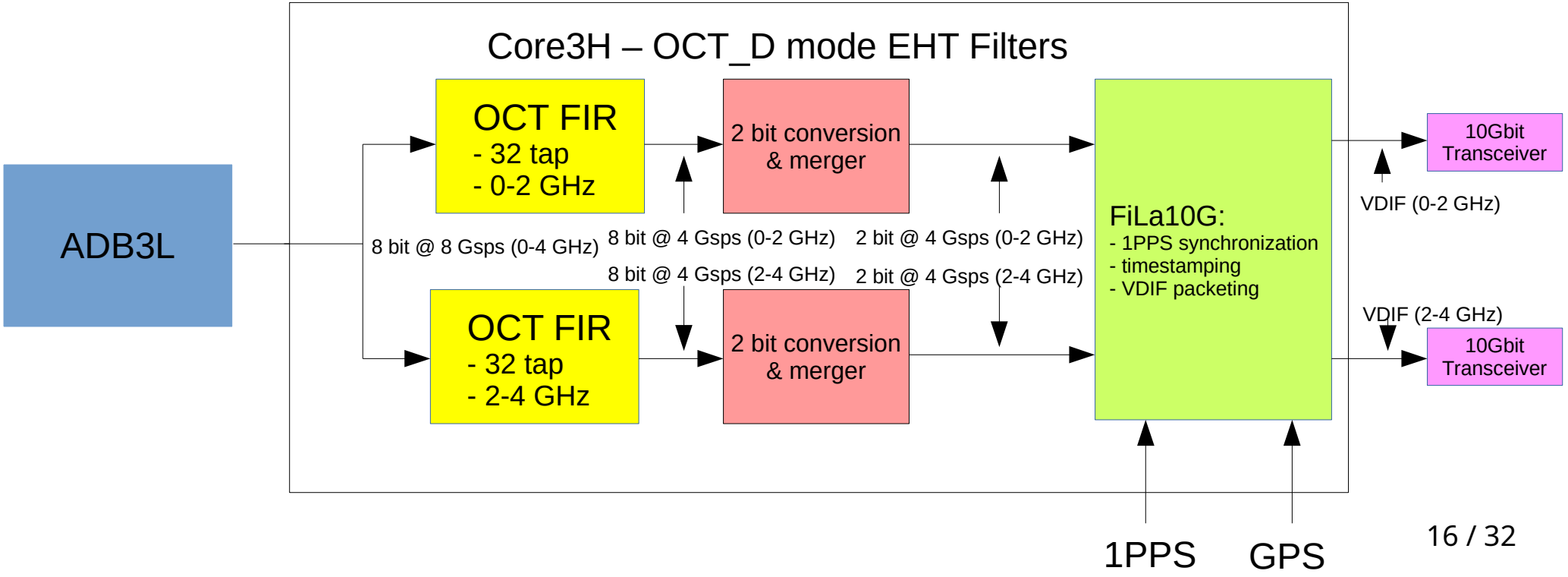
DSC-Mode

- Direct Sampling Conversion
- The full 4 GHz band is sampled, no additional filtering
- In 2-bit vdif-format it produces 16 Gbit/s datarate per IF
  → since the max. output datarate is 10 Gbit/s for each Ethernet-port, the vdif stream has to be split into four (4x4 Gbit/s) or two (2x8 Gbit/s) output streams
  → this requires reinterleaving the data after the recording to produce one vdif-file for the 4GHz channel



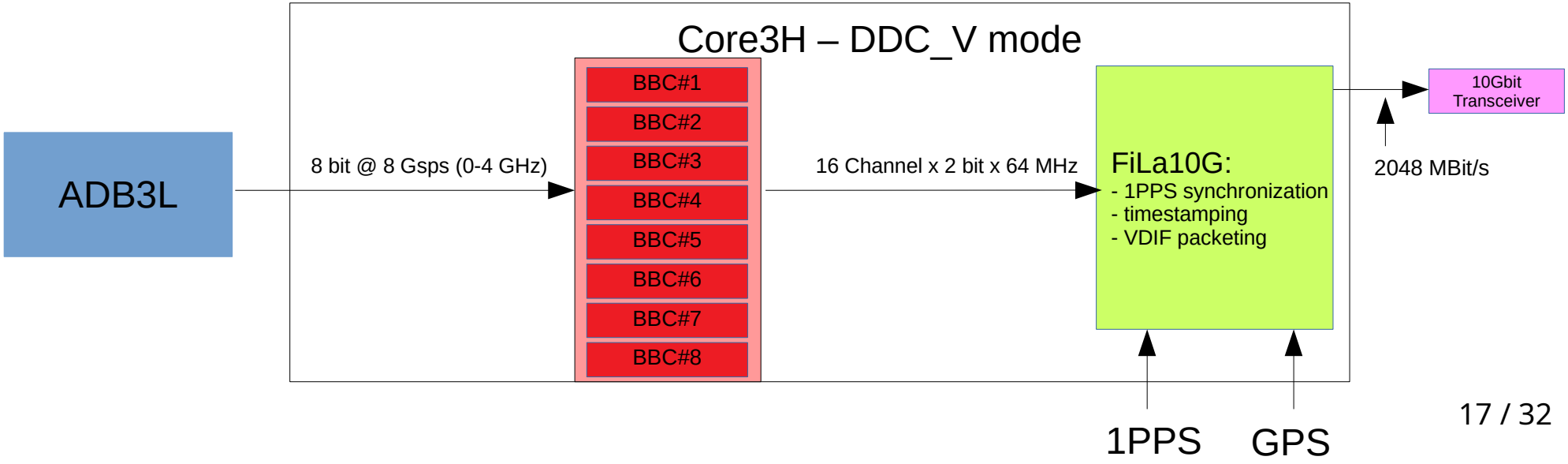
OCT

- Firmware provides one (OCT_S) or two (OCT_D) digital 32-tap FIR-Filters to filter subbands of 512, 1024 or 2048 MHz bandwidth.
- The filters can be loaded by the control software before the observation and even changed during runtime.
- The OCT_D mode using 0-2048 and 2048-4096 GHz filters is fully compatible with the R2DBE used in EHT observations.



DDC

- Digital Tunable Downconversion
- DDC_L (legacy): selectable bandwidth of 2, 4, 8, 16 and 32 MHz.
  Up to 16 BBCs/IF → max. 128 BBCs per System
- DDC_V (VGOS): 32 MHz filters with broader bandshape optimized for VGOS observations
  8 BBCs/IF → max. 64 BBCs per System
- DDC_U (unified): selectable bandwidth of 1, 2, 4, 8, 16, 32, 64 and 128 MHz.
  Up to 16 BBCs/IF → max. 128 BBCs per System
  under development



Configuration and Setup

- Control Software (in Folder C:\DBBC\bin):
  one for each mode: „DBBC3 Control_OCT_D_v110.exe“, „DBBC3 Control_DDC_V_v125.exe“,

- Config Files (in Folder C:\DBBC_CONF):
  - one main config file for each mode: „dbbc3_config_file_oct_D_110.txt“, „dbbc3_config_file_ddc_V_125.txt“
  - one config file for the ADB3L-Sampler settings „config_adb3l.txt“
  - for each Core3H a separate config file (for each mode): „ddc_V_core3H_1.fila10g“, „ddc_V_core3H_2.fila10g“, ...
  - (for DDC mode only): a config file with the BBC frequencies and BW: „config_ddc_V.txt“
  - (for OCT mode only): files with the filter taps: „0-2048_floating.flt“, „2048-4096_floating.flt“, „0-512_floating.flt“,...

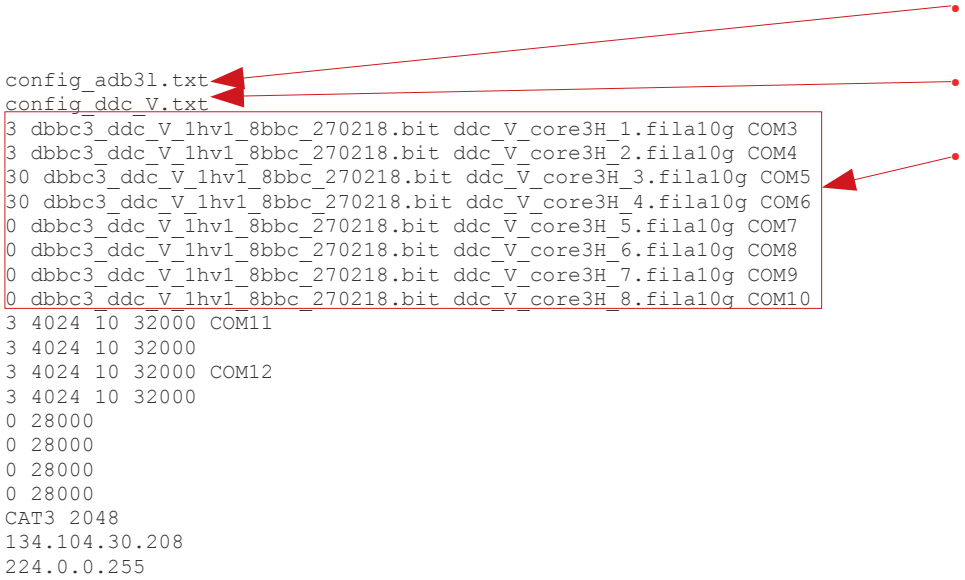
- Firmware (in Folder C:\DBBC_CONF\FilesDBBC):
  - one bit-File (FPGA-Firmware) for each mode: „dbbc3_oct_D_2hv2_250119.bit“, ...

- Documentation (in Folder C:\DBBC\manuals):
  - Command sets for Control Software, ADB3L and Core3H
  - Setup Procedures for the different modes
  - Changelogs for new versions

Control Software

- Loads the Firmware for the Core3H
- Starts the GCAT Clock Synthesizer
- Initializes and Synchronizes the ADB3L Samplers, loads settings for offset, gain, and delay.
- Initializes and configures the Core3H
- After initialization is finished, the control software provides a socket connection for communication using a socket client or the Field System.
- Through the control software direct communication with the GCoMo, ADB3L, Core3H and Synthesizer for the Downconversion is possible. A few examples:
  - core3h=1,time (check timestamp of the first Core3H-Board)
  - adb3l=offset=1,0,128 (set offset of the first sampler on the first ADB3L-Board)
  - synth=1,lock (check if the first LO-synthesizer is locked)
- Starting with DDC_V version 125 and OCT_D version 111, the control software supports multicast, for continuous monitoring of the system status by multiple clients. This gives out a multicast package every second with all the status information about the DBBC3. The Format of the Multicast package depends on the observation mode used, a description of the bit-pattern will be provided with the new software versions. Future graphical monitoring clients will use this feature.

Main Config-File



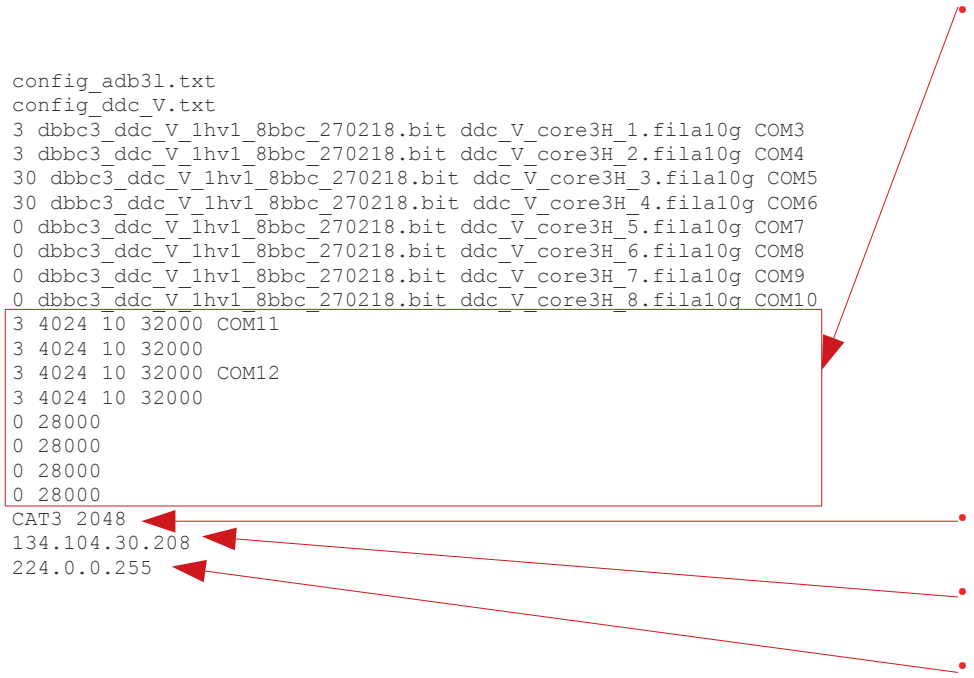
Config-file for Sampler settings

Config-file for BBC frequencies and BW (DDC only)

Configuration for Core3H-Boards:

- 3 dbbc3_....0218.bit ddc_V_core3H_1.fila10g COM3
  - 3 – board present and signal connected to IF
  - 30 – board present and no signal connected to IF
  - 0 – no board present
- 3 dbbc3_....270218.bit ddc_V_core3H_1.fila10g COM3
  - Firmware for the Core3H, located in the folder: „C:\DBBC_CONF\FilesDBBC“
- 3 dbbc3_....270218.bit ddc_V_core3H_1.fila10g COM3
  - Config-File for this Core3H
- 3 dbbc3_....270218.bit ddc_V_core3H_1.fila10g COM3
  - COM-Port for serial communication with Core3H

Main Config-File (2)



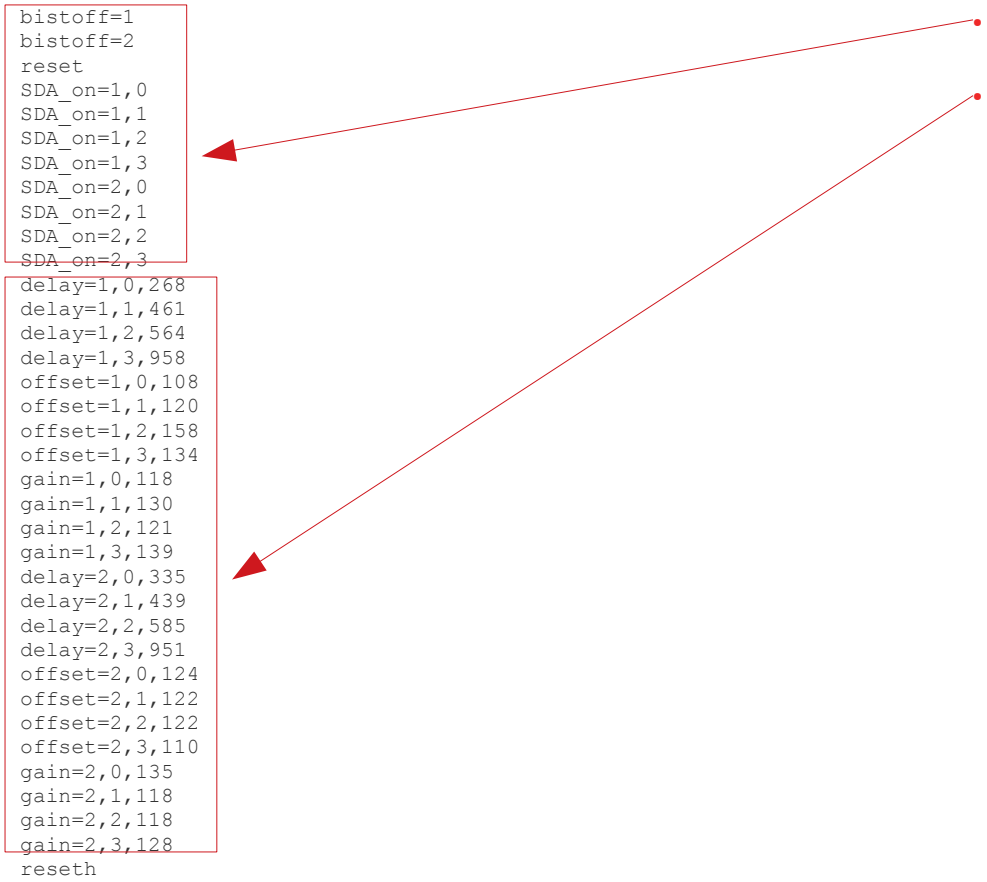
Configuration for GcoMos / Downconversion
- 3 4024 10 32000 COM11
  - 3 – GCoMo with internal synthesizer
  - 2 – GCoMo without internal synthesizer
  - 0 – No GCoMo present in that slot
- 3 4024 10 32000 COM11
  - synthesizer frequency (LO * 0.5)
- 3 4024 10 32000 COM11
  - synthesizer attenuation in dB
- 3 4024 10 32000 COM11
  - AGC target value
- 3 4024 10 32000 COM11
  - COM-Port for serial com. with synthesizer

GCAT Type and sampler clock frequency

The DBBC3s IP-Address in the network (for multicast)

IP-Address for Multicast-Group

ADB3L Config-File

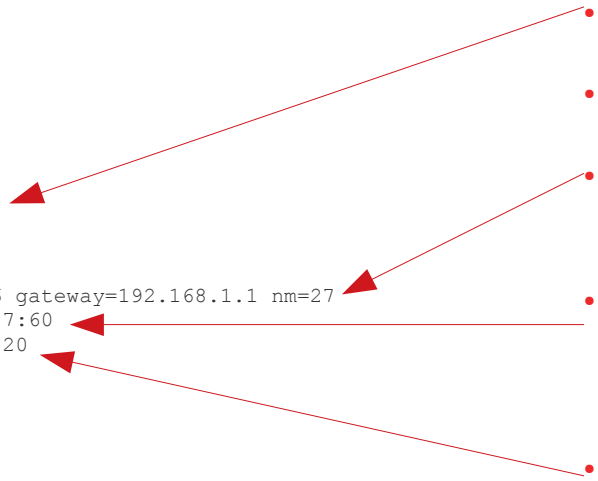


Static part

Calibration settings for each sampler
- format: command=board,sampler,value
- boards numbered from 1 to 8
- samplers numbered from 0 to 3
- range of values depend on the command
    - delay: 0-1023
    - offset: 0-255
    - gain: 0-255

Core3H Config-File (Example DDC_V mode)

```
core3_init
core3_mode pfb
regwrite core3 0 0x25252525
regwrite core3 1 0xBFBFBFBF
regwrite core3 9 1
reboot
inputselect vsi1
vsi_samplerate 128000000 2
splitmode off
vsi_bitmask 0xFFFFFFFF
reset
vdif_frame 2 16 8192 ct=off
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:44:47:60
destination 0 192.168.1.2:46220
timesync
start vdif
sysstat
```



- VDIF-Settings
- Ethernet Configuration:
- IP-Address, Gateway and Netmask for each Ethernet Port (1 in DDC, 2 in OCT and 4 in DSC)
- MAC-Address of Destination
  - second parameter is the LSB of destination IP-Address
- IP-Address of Destination

Additional Config-Files

- config_ddc_V.txt (for DDC-Mode only)
  - contains frequency and bandwidth for each BBC:

```
1  700.0 32
2  700.0 32
3  700.0 32
4  700.0 32
5  700.0 32
6  700.0 32
7  700.0 32
8  700.0 32
9  700.0 32
10 700.0 32
11 700.0 32
12 700.0 32
13 700.0 32
14 700.0 32
15 700.0 32
16 700.0 32
```

- Flt-Files with filter taps (for OCT mode only)
  - can be loaded with the control software after initialization:
  - tap=1,0-2048_floating.flt,1
  - tap2=1,2048-4096_floating.flt,1

```
-.101318359375000000E-01
0.103149414062500000E-01
-.342178344726562500E-02
-.317382812500000000E-01
-.254211425781250000E-01
0.101470947265625000E-01
0.147399902343750000E-01
-.272521972656250000E-01
-.482177734375000000E-01
-.206756591796875000E-02
0.438232421875000000E-01
-.220870971679687500E-02
-.922851562500000000E-01
-.623168945312500000E-01
0.145019531250000000E+00
0.358398437500000000E+00
0.358398437500000000E+00
0.145019531250000000E+00
-.623168945312500000E-01
-.922851562500000000E-01
-.220870971679687500E-02
0.438232421875000000E-01
```

Setup Procedure – General, for all modes

1) Make necessary changes to config-files:
   - main config-file: select the IFs that should be used, set the frequencies for the downconversion, …
   - Core3H config-files: configuration of the ethernet ports, correct MAC-Addresses, vdif_frame configuration, …

   → for DDC mode only: inputselect and vsi_samplerate could require adjustment:
   8 BBC firmware: inputselect vsi1
   12 and 16 BBC firmware: inputselect vsi1-2
   → the vsi_samplerate is determined by the used bandwidth of the BBCs:
   32 MHz → vsi_samplerate 128000000 2
   16 MHz → vsi_samplerate 128000000 4
   …
   - DDC-Config-File: adjust the frequencies and BW for the BBCs

2) Start the control Software for the required mode:
   - You will be prompted: `"Configure y/n? "`, press „y“
   - The firmware will be loaded and the system initialized
   - This can take some time, around 30 min for a system with full stack (eight IFs).
   - After the initialization and configuration the control software will be ready for a client to connect and starts to send the multicast packages

Setup Procedure – General, for all modes

3) Validate the system status:
   - Automatic: We provide python client scripts that perform all necessary validation steps and give feedback to the operator if something is wrong and what steps are necessary.
   → The checks include:
   - correct powerlevels for the IF inputs, verify that the GcoMos have enough dynamic range for automatic gain control
   - verify that the sampler clocks are correctly synchronized
   - verify that the 1pps is synchronized
   - verify time-synchronization
   - verify correct calibration of the ADB3L-boards (offset, gain, delay)
   - verify bit-statistics (18/32/32/18) distribution

4) Connect with Client Program or Field System

5) For DSC: System is ready for observation
   For DDC: perform additional tests
   For OCT: initialize filters

Setup Procedure – DDC mode

5) Check the frequencies and powerlevels of the individual BBCs, f.e. :
dbbc01 (for first BBC) gives the response:
dbbc001/ 250.000000,a,32,1,agc,52,36,14957,14932,0,0;

- the frequency and BW should be set as written in the config files, the power levels should be around 15k, the gain value should not be near 255 (the max gain value).

6) The system is now ready for observation

Setup Procedure – OCT_D mode

5) Load the filter coefficients (taps) for the FIRs:
   first Filter (output eth0): tap=1,0-2048_floating.flt,1
   second Filter (output eth2): tap2=1,2048-4096_floating.flt,1
   this has to be done for each Core3H-Board

6) Start the automatic loop for the threshold-control (2-bit conversion)
   enablecal=on,off,off
   enableloop

7) Check that the 2-bit conversion is working properly by checking the bit-statistics:
   core3hstats=1, core3hstats=2, ...
   The four distributions for each Core3H should all be around 18/32/32/18

8) The system is now ready for observation

Calibration

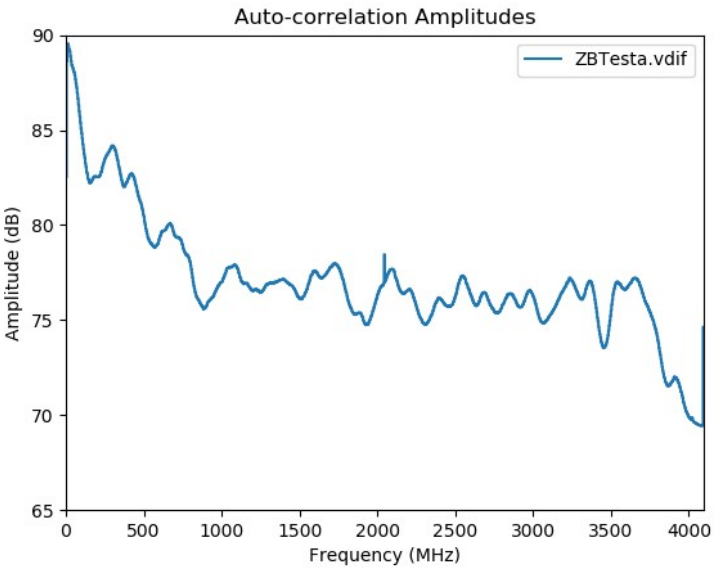
- The ADB3L uses 4-way interleaved sampling with four ADCs each running at 2048 MHz , providing a total bandwidth of 4096 MHz.
- This method requires a precise calibration of all four samplers on each board regarding offset, gain, and the time delay between them.
- Calibration requires a static 4 GHz noise source connected to the corresponding IF, the powerlevel should be between -20 to -15 dBm. -18 dBm is optimal. If a receiver is used as IF input, it must be in the same range as the noise source mentioned regarding BW and powerlevel, and remain static during the calibration!
- The Control Software provides commands that will perform the calibration and present the optimal values.
- These values should be compared and if necessary replace the values in the ADB3L-Config file.
- Usually recalibration is only necessary if the hardware has been modified, the values are stable between different runs.
- The order of calibration should always be offset, gain and last delay.

Offset-Calibration

- If the offset of the samplers is not properly calibrated, it will cause a characteristic tone in the middle of the spectrum at 2048 GHz. If this is visible, the offset-calibration should be repeated.
- The offset can be checked by looking at the corresponding bit-statistics, visible with
  core3h=1,core3_bstat 0
  for example. The distribution of the sign bit should be 50%/50% with a 1-2% margin acceptable.
- To perform the calibration:
  Set the corresponding GCoMo to high attenuation, f.e. dbbcifa=2,60, so that the power values are between 5k and 10k. With these relatively low values the offset-calibration is more precise.
- Issue the offset-calibration with the command:
  cal_offset=board_nr
  where board_nr is the number of the ADB3L from 1 to 8
- After the calibration the correct offset-values are set and should be copied into the ADB3L config-file for the next run.

Example for bad offset:
core3h=1,core3_bstat 0
gives the bit statistics of the first sampler (first board):

```
CORE3 input bit statistics of sampler 0:
P("11") = 20.39% (13050705)
P("10") = 31.79% (20346379)
P("01") = 30.39% (19454264)
P("00") = 17.41% (11148652)
```



Gain-Calibration

- All four samplers of an ADB3L board get the same analog signal, so to prevent artifacts they should all have the same power level, within <1% margin.
- The gain-calibration is performed with the default powerlevels in the GCoMo, meaning the automatic gain-control should be turned on (dbbcifa=2,agc) and the nominal power target of 32k should be reached.
- The calibration is performed with the command: cal_gain=board_nr (board_nr from 1-8)
- After the calibration the correct gain-values are set and should be copied into the ADB3L config-file for the next run.

Example for bad gain:
core3h=1,core3_power
gives the power values off all four samplers of one board:

```
core3_power
CORE3 input bit statistics:
  Power at sampler 0 = 824390312
  Power at sampler 1 = 741771007
  Power at sampler 2 = 745231277
  Power at sampler 3 = 742251194
```

Delay-Calibration

- The time-delay between the four samplers on the ADB3L-Board need to be 90° as precise as possible, to allow the interleaved sampling method to work correctly.
- This time-delay is already roughly adjusted on the PCB, but a fine-adjustment with calibration is necessary for maximum precision.
- The calibration measures the exact delay between the samplers using an on board cross correlation and determines the correct delay values with a precision of about 0.2 ps.
- The setting for the corresponding GcoMo is the same as in the gain-calibration, agc at 32k power reached.
- The calibration is performed with the command: cal_delay=board_nr (board_nr from 1-8)
- After the calibration the correct delay-values are set and should be copied into the ADB3L config-file for the next run.

- Example of good delay calibration:
  checkphase
  checks calibration, values should be close to 255M:

```
...
Board 1:
253514567
253752991
254228977
```

- Example of bad delay calibration:

```
...
Board 1:
232659866
253752143
254239556
```