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To:EDGES GroupFrom:Alan E.E. RogersSubject:Defects in ADCs evident in long integrations

Converting radio signals from analog to digital as early as possible in the receiver chain may not always be the best approach for very weak signals. The narrowband system of the deuterium array was able to integrate down for years before reaching instrumental limits at levels of a few parts per million of the total power or an equivalent dynamic range approaching 120 dB. On the other hand wideband direct sampling systems from industry are full of spurious signals and may not even reach a spurious free dynamic range (SFDR) of 60 dB. Figure 1 shows the spectrum from an AC240.

In addition to the spurs from clock frequencies and sub-harmonics of the sample clock these wideband systems also exhibit a much more insidious problem which produces ripples and steps in the bandpass. Figure 2 shows an expanded view of the spectrum showing the hidden structure of the bandpass from 100 to 200 MHz.

The discrete frequency spurs are usually reasonably constant so that Dicke switching between signal and comparison results in cancellation of the spurs in the difference spectrum as shown in figure 3. However, the ripples and steps will only cancel out if the signal and comparison spectra are very close in shape and total power see figure 4. Double Dicke switching in which an artificial spectrum generator is alternately substituted for the signal being analyzed can reduce the steps and ripple but it is not possible to make an accurate artificial spectrum for EDGES because the sky spectrum varies with the orbits of the satellites whose downlinks occupy the 100-200 MHz band of interest. The exact cause of the steps and ripple is difficult to determine as the manufacturers are unwilling to divulge the details of their circuit boards.

Software simulations show that any coupling between the digital output of the ADC and its input or any mechanism which influences the selected digital state of the ADC causes ripple in the spectrum. The period of the ripple is the inverse of the digital delay. Steps in the output can be the result of aliasing with spurs or sub-harmonics of the sample clock. The FPGA clock is a sub-harmonic of the sample clock and a step in the output occurs at this frequency. Changing the sample frequency moves this step and influences its amplitude. The analog bandpass has little effect on the magnitude of the step when expressed in degrees K from the calibration. Some improvements in performance were made by using an external source for the sampling clock and changing the sampling frequency to minimize the ripple and steps. The best performance obtained so far using the AC240 is at a sample rate of 910 MHz. The systematics in switching between a 300 K load and a sky noise simulator are now at about 50 mK peak to peak in the range 110 to 200 MHz as shown in figure 5.

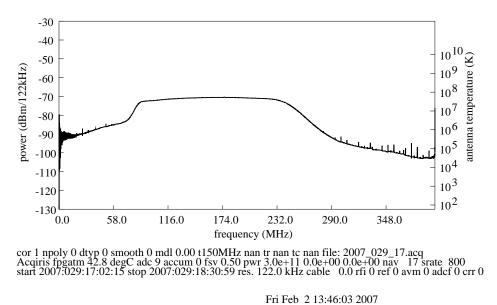
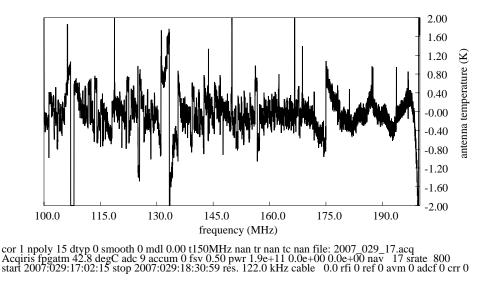


Figure 1. Spectrum of noise source from AC240 with 800 Ms/s. Note the spurs and steps in the spectrum beyond the edge of the analog filter at about 280 MHz.



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Figure 2. The spectrum from 100 to 200 MHz of the data in figure 1 after the removal of a polynomial. The vertical scale is now expanded to a linear temperature.

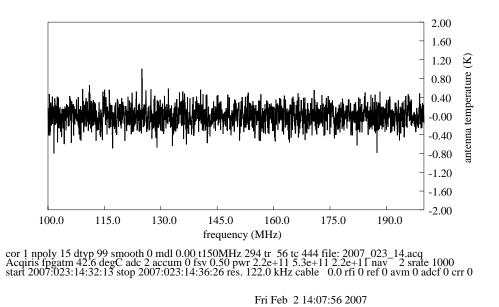


Figure 3. The difference spectrum between antenna and load at the same temperature.

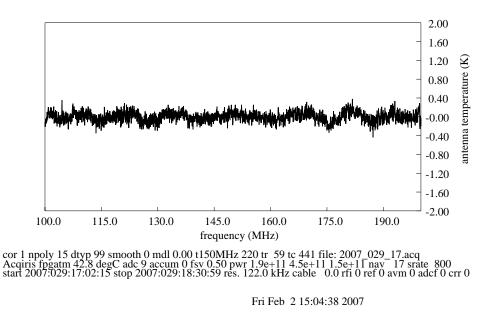


Figure 4. The difference spectrum between antenna and load at different temperatures. Many of the residuals correspond to the details in figure 2.

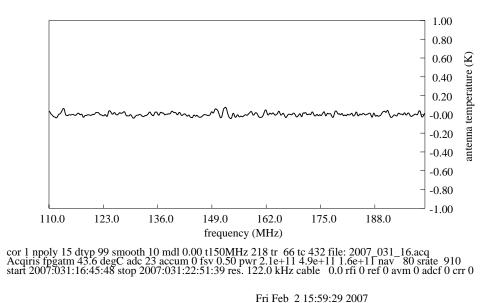


Figure 5. 6 hour integration with spectrum smoothed to 1 MHz resolution. Note the systematic around 150 MHz and another close to 112 MHz.