MASSACHUSETTS INSTITUTE OF TECHNOLOGY
HAYSTACK OBSERVATORY

12 May 2000

TO : Mark IV Development Group

FROM : Dan Smythe

SUBJECT : Preliminary Evaluation of a Gigabit-Rate Chip Set for Data Communication (G-Link)

Hewlett-Packard has developed and is marketing the HDMP-1000 G-Link transmit/receive chip set as a "transparent" ribbon cable replacement at data rates up to 1167 Mb/s (1367 Mb/s if the case temperature can be kept below 55°C). Although designed for full-duplex applications, it is possible to configure it for simplex applications such as video distribution, as described later.

In our application, with the addition of a 32:16 multiplexer, the link would carry 32 data bits, plus two clocks (32 and 64 MHz), and two control bits, over a single coaxial cable at 1280 Mbaud. At a case temperature below 55°C, it could handle 40 data bits. Each station unit would require two transmitters to handle the 16 bits each of sign, magnitude, and validity, with 16 bits left over. With the Bos architecture, each correlator board would require 6 receivers to handle the 3×64 bits of input. In addition, we would need to distribute the output of each transmitter to as many as 5 receivers. This distribution system would require video power dividers and amplifiers with frequency response flat from 64 to 1280 MHz.

Bit-error-rate performance is better than 10^{-10} using RG-58 coax shorter than 22 meters, and error checking is minimal. Isolated errors, although reported, are ignored by the link; so that in our application the link should stay synchronized as long as power is applied to both transmitter and receiver. If two consecutive errors are detected, the receiver will require a few milliseconds to resynchronize. If each receiver is provided with a 64-MHz phase-modulated oscillator, this time could be reduced to a few microseconds.

Simplex operation is made possible by providing each receiver with an external 64-MHz clock. This clock could be supplied by transmitters in the data distributor by running one additional coaxial cable from the data distributor to each correlator module. The receivers in the Data Distributor could get their 64 MHz clocks from the output transmitters.

Alternatively, the Correlator Control Computer could ask one or more of the transmitters to send fill frames whenever too many errors are detected. This mode of operation would eliminate the need for the external 64-MHz clock to the receivers, since the receivers normally synchronize on fill frames. The receiver has 3 different output status lines than can be used by the Correlator Control Computer to monitor the performance of the link.

All internal signals are differential to improve noise margin and to reduce ground currents, which could disrupt the analog circuitry. As a consequence, the transmitter has two sets of complimentary 50-ohm outputs—the normal serial data output, and a loop-back output—with one pair or the other active depending on the state of a control signal. We might be able to take advantage of these extra outputs, since the loop-back feature is not used in a simplex link. Similarly, the receiver has complimentary serial inputs.

These chips require a -5-volt power supply, typically 340 mA for the transmitter and 427 mA for the receiver; and each receiver requires -2 volts at 0.17 A for ECL pull-down terminations. This requirement adds up to -5V @ 1 A for each station unit, and -5V @ 2.5A plus -2V @ 1A for each correlator board. This power budget does not include power for the 32:16 multiplexers, re-clocking flip-flops, and video distribution amplifiers.

Delays in these chips are typically 1 or 2 ns, so that the timing of signals from multiple links with identical lengths of coax should be better than that, but a definitive answer to this question will have to wait until we get some chips for evaluation. We have ordered two evaluation boards for delivery in a few weeks.

These chips are priced around $200 in the quantities that we anticipate using in the Mark IV correlator, and delivery is 6 weeks.