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SUBJECT: Correlator-Board Backplane-Interface Signal Requirements

Abstract

This memo defines the purpose, characteristics and required timing of all signals required at the correlator-board backplane interface, exclusive of all VME related system signals.

Discussion

The correlator board is fundamentally driven by the following externally-generated signals:

CBCLOCK (Correlator Board Clock)

Purpose:

Fundamental clocking signal for correlator board. All synchronous activity on the correlator board is driven by CBCLOCK.

Comments:

The CBCLOCK signal is continuous and at a constant frequency corresponding to the highest-allowed sample rate (32 MHz for VLBI; 53 MHz for SMA; 40 MHz for Westerbork). Synchronous signals are required to be well defined at the rising edge of CBCLOCK, which means they meet the setup and hold requirements with respect to the CBCLOCK transition from the lower logic level to the higher logic level.

DATA (Sign, Magnitude, Validity)

Purpose:

Sign and Magnitude signals are data to be correlated. The Validity signal can be asserted on a sample-by-sample basis in certain modes to filter out bad data or to process special modes. Note that there are 64 data channels (192 signal wires) at the board. The description here is in terms of a generic signal "DATA" whose behavior is common to all the 64 data signals. The

Validity signal-line is also used to carry dynamic-parameter data during BOCF.(Synchronous signals. The code is specified in the following table)

Sign	Mag	Val	Meaning
0	0	0	Illegal input
0	0	1	+1
0	1	0	Invalid Sample
0	1	1	+3
1	0	0	Invalid Sample
1	0	1	-1
1	1	0	Invalid Sample
1	1	1	-3

Comments:

The Validity signal is not available to control processing in the 4x4 (SMA) mode.

For 1-bit data, the Magnitude bit should always be held to logical '1'. This will facilitate the optimal processing of cases where 1-bit data must be correlated against 2-bit data.

The Validity signal may also be used to facilitate certain special data-processing modes, such as pulsar gating.

BOCF (Beginning of Correlator Frame)

Purpose:

The leading edge of BOCF defines the beginning of the Correlator Frame and, by implication, the first sample of the Correlator Frame (though actual correlation is blanked for the duration of the BOCF). While BOCF is being asserted, up to 240 bits of dynamic-parameter data may be captured from the validity-signal-line by an internal correlator-chip buffer. Actual correlation is enabled at the first data-sample following the trailing edge of BOCF; the initial conditions of the on-chip phase-rotator and vernier-delay generators are also applied to this sample. (Active high, synchronous signal)

Comments:

By convention, there are always an integral number of CF's per Reconstituted Observe Time (ROT) second, and the phasing of CF's will be such that the leading edge of BOCF always fall on the (ROT) second tick.

For applications not using the header capture within the chip, the BOCF may be as short as TBD1 clock cycles. For applications not using dynamic parameters, the BOCF may be as short as TBD2 clock cycles. This is the time required for internal management of chip function between correlator frames.

SHSMP (Shift Sample)

Purpose:

Causes data to be shifted one position in the correlator shift registers. This is primarily useful in discarding samples from over-sampled data. During BOCF, also causes a bit to be captured in the chip header -buffer. Recall that, during BOCF, header data always occurs at the data-sample rate. If the data-sample rate to the correlator board is less than the CBCLOCK rate, the use of SHSMP is required to filter out 'duplicate' header bits. (Active high, synchronous signal)

Comments:

SHSMP can be generated in two different ways, the choice being made by the action of an initialization protocol via the VME bus. It can then be generated by control logic on the correlator board, or it can be generated by the board interface signal ENSHFT. ENSHFT has a delay of two clock cycles in its path when it is allowed to cause SHSMP.

For some cases of processing oversampled data, it is necessary that SHSMP be set to a different divide ratio (with respect to CBCLOCK) during BOCF and outside of BOCF.

Although SHSMP may be provided to the correlator board as an external signal, provisions have been made on the correlator board for internal generation of SHSMP in the ratio of 1, 2, 4, 8 and 16 to CBCLOCK. For this internal generator, the divide ratio of SHSMP may be set independently during BOCF and outside of BOCF. The phasing of the internally-generated SHSMP is *always* such that it is referenced to the *rising* edge of BOCF, i.e. the trailing edge of BOCF has no effect on the phasing of SHSMP following BOCF. This guarantees that the epoch of the correlated samples remains stable for different divide-ratios of SHSMP and for various lengths of BOCF.

ACCUM (Correlator Accumulate)

Purpose:

Enable correlator accumulators on sample-by-sample basis. The primary use of ACCUM is to prevent accumulation during BOCF, although ACCUM may also be used for some special purposes. (Active high, synchronous signal)

Comments:

ACCUM can be generated in two different ways, the choice being made by the action of an initialization protocol via the VME bus. It can then be generated by control logic on the correlator board, or it can be generated by the board interface signal ENADD. ENADD has a delay of two clock cycles in its path when it is allowed to cause ACCUM.

ACCUM is normally de-asserted during BOCF to stop accumulation during this period. Special processing modes can be facilitated by using ACCUM to gate the period of actual accumulation.

Although ACCUM can be provided to the correlator board as an external signal, provisions have been made on the correlator board for internal generation of ACCUM in the ratio of 1, 2, 4, 8 and 16 to CBCLOCK. This allows higher-precision correlation on data being shifted through the correlator at rates less than CBCLOCK. The divide ratio of ACCUM is set independently of the divide ratio of SHSMP. ACCUM is always inactive during BOCF so as

not to accumulate any header data. The phasing of the internally-generated ACCUM is always such that it is referenced to the rising edge of BOCF in the same way as SHSMP. Although ACCUM is normally de-asserted during BOCF, it is possible (under DSP control) to ignore BOCF; this is potentially useful in cases where the Validity signal is being used only to transmit header data to the correlator chip and does not indicate the validity of the data.

LOADB (Load Buffer)

Purpose:

LOADB causes the contents of the ripple counters to be loaded into the buffer registers. The prior contents of the buffer registers are over written. (Active high, asynchronous. Minimum activation time is TBD ns.)

Comments:

LOADB can be generated in two different ways, the choice being made by the action of an initialization protocol via the VME bus. It can then be generated by control logic on the correlator board, or it can be generated by the board interface signal TRDATA. TRDATA has a delay of two clock cycles in its path when it is allowed to cause LOADB.

This signal should only be asserted when the ripple counters are stable (not propagating any carries).

CLRC (Clear Counter)

Purpose:

This signal causes the ripple counters to be set to a count of zero. (Active high, asynchronous. Minimum activation time is TBD ns.)

Comments:

CLRC can be generated in two different ways, the choice being made by the action of an initialization protocol via the VME bus. It can then be generated by control logic on the correlator board, or it can be generated by the board interface signal CLEAR. CLEAR has a delay of two clock cycles in its path when it is allowed to cause CLRC.

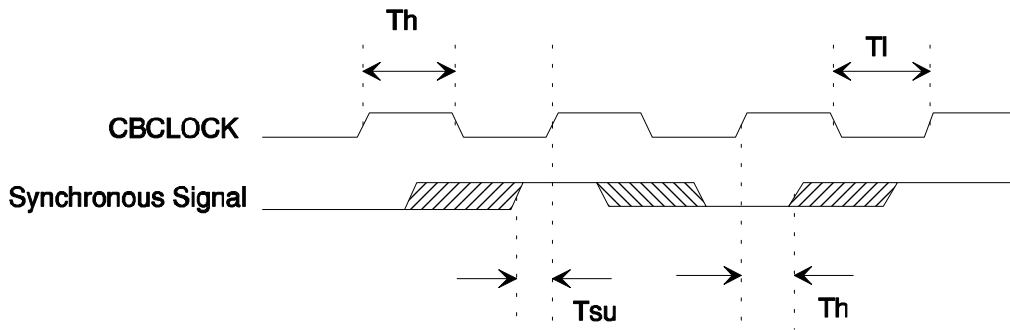
This signal is normally used to clear the counters (which constitute the 24 most significant bits of the accumulators) just after their contents have been transferred to the buffer registers. This signal has no effect on the contents of the three least significant bits of the accumulators and does not alter the contents of any of the sample registers.

Signal Sequencing

This section describes the requirements of synchronous signals and gives examples of typical operational sequences.

Synchronous Signals

The figure below shows the required timing relation between synchronous signals and the signal CBCLOCK:



The limits on the parameters shown in the diagram above are given in the following table.
 (The frequency range of CBCLOCK is from 15 to 64 MHz.)

Parameter	Min	Max	Units
T_h	8	58	ns.
T_l	8	58	ns.
T_{su} (data)	1	-	ns.
T_h (data)	2	-	ns.
T_{su}	TBD	-	ns.
T_h	TBD	-	ns.

The following figure, entitled "Typical VLBI Sequencing" is presented to give a high level description of VLBI processing *as observed at the correlator chip pins*. (The relation of chip timing to board connector timing is straightforward and is shown later.)

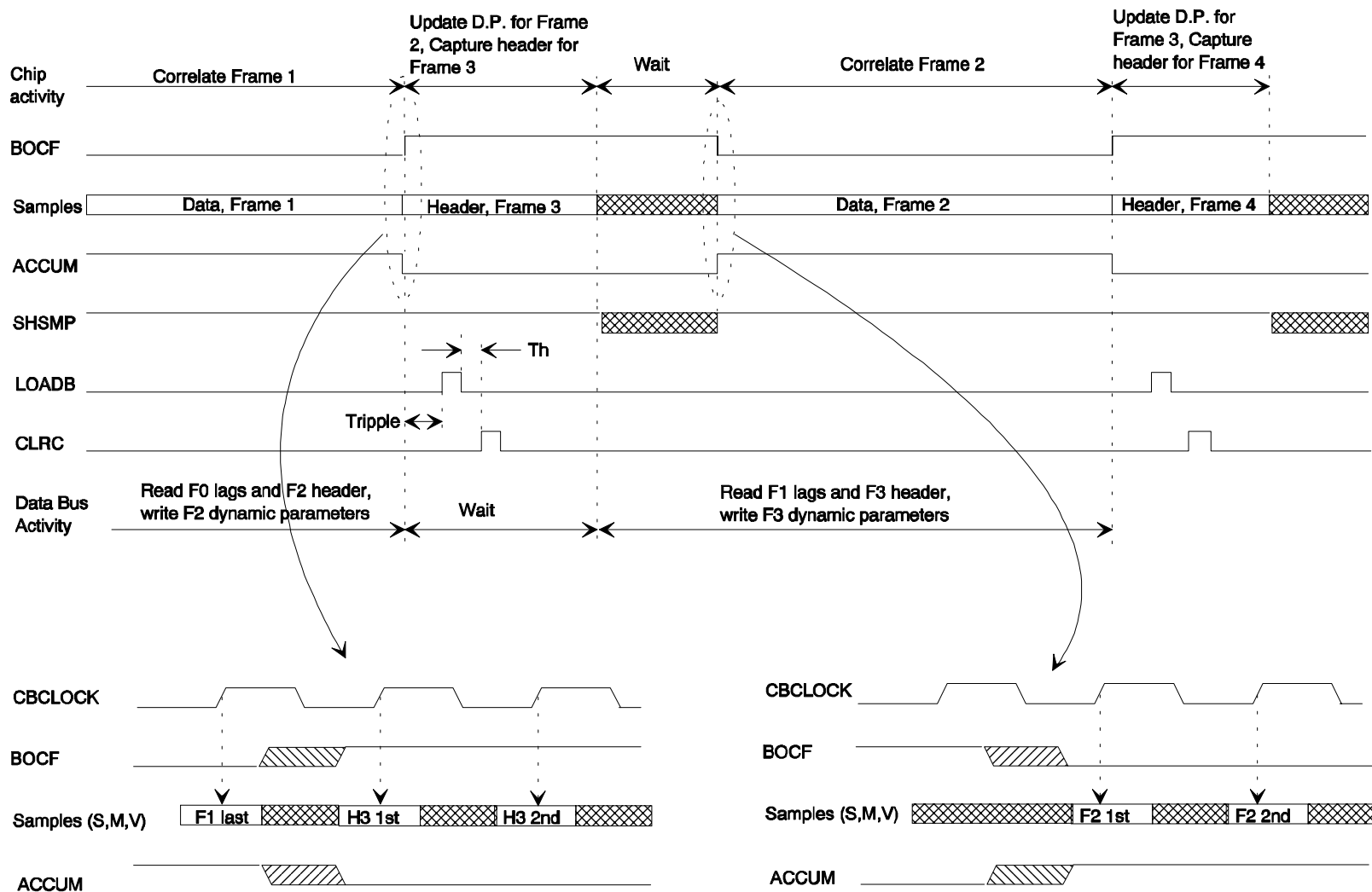
VLBI processing means that the header capture feature and the dynamic parameters are in use. (All applications are expected to specify the static parameters which are not referenced here.) The figure shows "steady state processing" which is assumed to continue in the same sequence for a number of correlator frames. The figure is not to scale in the sense that the data in a frame would be expected to be very much longer than the duration of a BOCF pulse.

The top row of the diagram gives a running commentary on the activity inside each active chip on the board. The signal BOCF is shown explicitly, and its synchronous relation to the data signals (collectively referred to as Samples) and to CBCLOCK and ACCUM are shown in the detailed expansions in the vicinity of changes in BOCF.

The diagram opens with the correlation processing of frame 1. During this time, a parallel operation is taking place which is governed by the on board DSP. This activity takes place through the medium of the data bus which is an independent channel between the DSP and the correlator chip array. During the correlation of one frame, the DSP reads the results of the

prior frame, reads the header(s) which have been "captured" (stripped out of the sample stream during the prior BOCF), computes the dynamic parameters to be used for the next frame, and loads the dynamic parameters for the next frame. All these tasks must complete during the time of correlation of the current frame.

At the rising edge of BOCF, the mode of operation of the chips changes. The accumulators stop operating as caused by the falling of ACCUM, and the data stream is assumed to contain header information which starts to be captured at the rising edge of BOCF. A carry might have been initiated in the ripple counters which form the upper stages of the accumulators on the last sample, so adequate time for the carry to ripple to completion must be allowed before the signal LOADB is asserted. This signal causes all of the accumulator and count values to be



Typical VLBI Sequencing

loaded into the 24 bit buffer registers, overwriting any previous contents. (Which is why the previous results must have all been read out by his time.) Once the new results have been transferred to the buffer registers, the LOADB signal is de-asserted and after an appropriate delay (T_h) the signal CLRC is asserted to clear the upper 24 bits of the accumulators. The correlation process could then begin again, but two other parallel operations, the header capture, and the dynamic parameter update must first be completed.

Header capture requires the input of 240 samples, so this translates to a minimum wait of 240 periods of CBCLOCK. At the same time the previously-written dynamic parameters are updated into the phase generators and delay trackers, a somewhat faster operation as all blocks update simultaneously and each block has only 21 parameters of 16 bits each. Once these operations are concluded, the chip is prepared to commence correlation of the next frame when BOCF goes to "0".

Note that the onset of readout of lags can begin as soon as the headers are captured. There is no external signal to the DSP to indicate this, so a reasonable behavior of the DSP would be to wait for the fall of BOCF to begin this operation.

Some of the flexibility of the operation of the signals ACCUM and SHSMP is shown in the following figure entitled "Hypothetical Processing Example". In addition, the details of the relation of board timing to chip timing is shown.

In order to make the sequence diagrams fit into a document of reasonable proportions, the figure presents the situation where the header consists of 16 bits and the first five samples are labelled A, B, C, D, and E. We assume here that the data input rate is the same as the CBCLOCK rate and that the data samples are replicated four times.

The first item to note is the relation between BOCF at the board connector and BOCF as it is presented to the correlator chip pins. There is a two-clock-period pipeline delay. This delay applies to data Samples as well as to control signals. The data sample pipeline is contained in the crosspoint switches. The control signal pipeline is contained in on-board logic.

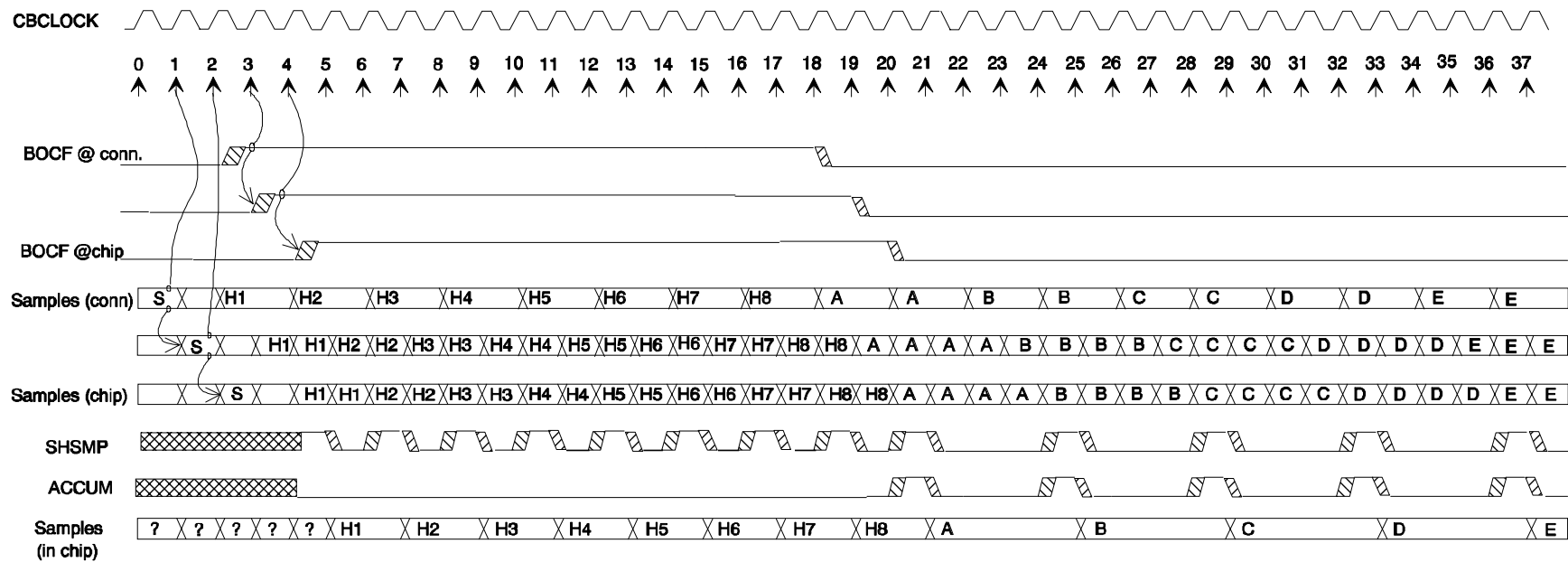
The signals SHSMP and ACCUM are not shown with the pipeline delay because the figure refers to the case where they are generated internally within the board. Note that in the example SHSMP is asserted throughout BOCF (divide by 1) and is asserted every fourth sample thereafter (divide by 4). The result is that all 16 header bits are captured, and each of the data samples are entered singly. Note also that the signal ACCUM behaves somewhat differently from the previously shown overview in that it accumulates twice per sample entered. This will cause the accumulated values to be twice as large as they would have been if they were accumulated once per sample.

A slight variation on the hypothetical example is shown on the figure on the following page. In this case we assume that the sample data all enters the board at 1/2 CBCLOCK rate. (Once again to fit the page we make the convenient assumption that the header now consists of eight bits.) For some reason, the data samples are each duplicated in the incoming data stream.

In this case, the proper processing can take place if SHSMP is set to divide by 2 during BOCF and to divide by 4 during correlation. Each lag is to be accumulated once, we assume, so ACCUM is set to mimic SHSMP during correlation and it also divides by 4.

In general, there are three independent division constants which can be set into the board to control the rates of SHSMP and ACCUM. Each of these constants can have value 1,2,4,8, or 16. The division rates of SHSMP during BOCF and during correlation are independently specified. The third constant specifies the division constant for ACCUM.

Although ACCUM has been shown inactive during BOCF in all the example sequences, there is a mode in which ACCUM can be kept active during BOCF. This is a somewhat degenerate mode in which the correlation proceeds right through the header capture process, but the samples are considered unconditionally valid because the validity bit is carrying header data and cannot affect processing.



Hypothetical Processing Example
Samples at 1/2 CBCLOCK rate