MASSACHUSETTS INSTITUTE OF TECHNOLOGY
HAYSTACK OBSERVATORY

CORRELATOR BOARD
HARDWARE SPECIFICATION

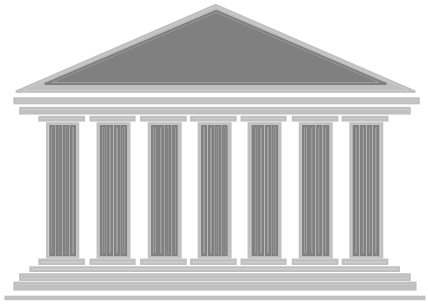

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TABLE OF CONTENTS

1.0 Introduction

This document details the technical hardware and software control specification of a new high speed correlator board for processing signals used in radio astronomy. It supports both Connected Element and VLBI modes of operation. Thirty-two VLSI Correlator ASIC's [2] are incorporated in the design of the board. Some of the board processing capabilities are:

- 16,384 real lags at 64 Mega-Samples/second

- 4,096 real lags at 256 Mega-Samples/second using a 4 x 4 correlator array

- Flexible configuration to support many operating modes, including VLBI 120 baselines at 32 Mega-Samples/second, 32 complex lags/baseline

- Array of cutsom high speed 64 x 64 XBAR switches to route data to correlator ASIC inputs

- Test RAM for injecting simulated VLBI data through correlators

- Buffer capture of signals from backplane to examine data integrity

The board has resident processing capability in the form of two TMS320C40 microprocessors, which program, process and unload correlator data.

1.1 Related Documents

[1] "Mark 4 Processor Real and Complex 4x4 Cell Usage Block Diagram" J.Levine, 18-May-93

[2] "The Haystack VLSI Correlator Chip" A.Whitney, W. Aldrich, 10-June-1993

[3] "Internal Technical Report 202, The EVNFRA Correlator : Design Considerations" A. Bos, March - 1993

2.0 General Objective

The objective of this document is to introduce the reader to a comprehensive overview of the Mark 4 correlator board operation. This document complements [2]. Section 3 presents a high level hardware description of the correlator board, section 4 will cover board programming, and section 5 details power requirements and mechanical considerations.

3.0 Hardware Specifications

The correlator board is VME based measuring 12U x 400mm. Figure 1 represents the hardware block diagram of the board.

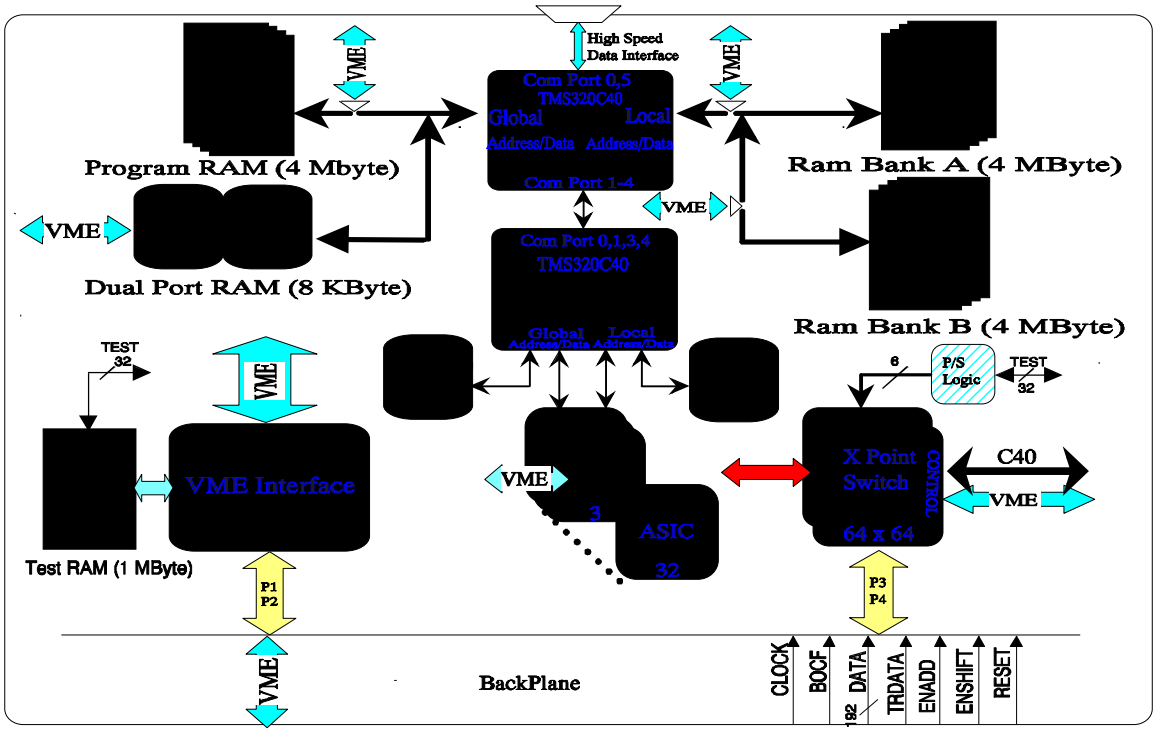


Figure 1

3.1 External Interfaces

Four connectors varying in pin count will pass signals into and out from the correlator board. The standard 12U VME designation for these connectors is P1, P2, P3 and P4. Connector P1 and P2 are 96 pin DIN style connector. Connector's P3 and P4 are 160 pin DIN style connectors. P1 and P2 pass system defined VME/VXI signals. One hundred and sixty pins on P3 and P4 for a total of three-hundred-twenty pins are user defined.

3.1.1 VME Interface

The correlator board will reside as a slave in VME extended address space (A32) and respond to address modifier codes 09, 0A, 0D and 0E Hex. ***Only*** longword (D32) accesses are permitted. The correlator board ***will not*** respond to word (D16) or byte (D8) access. The board will support VME block transfers with address modifier codes 0B and 0F Hex.

The correlator board generates one vectored VME bus interrupts. A VME bus master programs the level and associated vector. Events generating VME bus interrupts are initiated when the C40 processor access one memory location in Dual Port RAM.

3.1.2 User Defined Pins

The following signals which are transmitted via VME bus connectors P3 and P4 are common to all collaborative parties.

BOCF	Beginning of Correlator Frame
CLOCK {COAX}	Data Clock on the board
DATA - Validity {Pin Count : 64} - Sign {Pin Count : 64} - Magnitude {Pin Count : 64}	Correlation data from Cross Point Switch Note: For **SMA** applications, there are **96 Sign and Magnitude** data inputs.

The following signals are allocated for NFRA applications.

ENADD {Pin Count : 1}	Enable Accumulators
ENSHIFT {Pin Count : 1}	Enable Data Shift Registers
TRDATA {Pin Count : 1}	Transfer Data From Accumulators to Readable Buffers
CLEAR {Pin Count : 1}	Reset the Accumulators

For ***non*** EVN applications, ENADD, ENSHIFT, TRDATA and RESET are terminated from the drivers side to ground. All signals are transmitted single ended with TTL or CMOS logic levels through connectors P3 and P4 with the ***exception*** of the CLOCK. The CLOCK is transmitted with TTL (or CMOS) logic levels through a coaxial cable to a ***Coaxial*** style connector. Four other *high current* coaxial connectors carry two VCC's and two GND's. On P3 and P4, the two outer columns will carry signals, while the middle column will carry signal returns. Chassis ground is tied to pin E32 on connector P4.

3.1.2.1 User Defined Pinout

J3	A	B	C	D	E
1	BOCF	PTRDATA	GND	PCLEAR	PENADD
2	ENSHIFT	SPARE_A1	GND	SPARE_A2	SPARE_A3
3	A_Sign 4	GND	GND	A_Sign 9	A_Sign 15
4	A_Sign 17	A_Sign 5	GND	A_Sign 10	A_Sign 16
5	GND	A_Sign 11	GND	GND	GND
6	A_Sign 7	A_Sign 12	GND	A_Sign 18	A_Sign 6
7	A_Sign 8	A_Sign 13	GND	A_Sign 3	A_Sign 19
8	A_Sign 27	GND	GND	A_Sign 2	A_Sign 14
9	A_Sign 28	B_Sign 2	GND	A_Sign 20	A_Sign 1
10	GND	A_Sign 21	GND	GND	GND
11	B_Sign 4	A_Sign 22	GND	A_Sign 29	B_Sign 3
12	A_Sign 31	B_Sign 5	GND	A_Sign 23	A_Sign 30
13	A_Sign 32	GND	GND	B_Sign 6	A_Sign 24
14	A_Sign 26	B_Sign 7	GND	B_Sign 8	A_Sign 25
15	GND	B_Sign 1	GND	GND	GND
16	B_Sign 10	B_Sign 14	GND	B_Sign 19	B_Sign 9
17	B_Sign 21	B_Sign 11	GND	B_Sign 15	B_Sign 20
18	B_Sign 22	GND	GND	B_Sign 12	B_Sign 16
19	B_Sign 18	B_Sign 23	GND	B_Sign 13	B_Sign 17
20	GND	B_Sign 25	GND	GND	GND
21	B_Sign 26	B_Sign 27	GND	B_Sign 32	B_Sign 24

22	B_Sign 31	B_Sign 30	GND	B_Sign 29	B_Sign 28
23	A_Valid 4	GND	GND	A_Valid 9	A_Valid 15
24	A_Valid 17	A_Valid 5	GND	A_Valid 10	A_Valid 16
25	GND	A_Valid 11	GND	GND	GND
26	A_Valid 7	A_Valid 12	GND	A_Valid 18	A_Valid 6
27	A_Valid 8	A_Valid 13	GND	A_Valid 3	A_Valid 19
28	A_Valid 27	GND	GND	A_Valid 2	A_Valid 14
29	A_VAlid 28	B_Valid 2	GND	A_Valid 20	A_Valid 1
30	GND	B_Valid 3	GND	GND	A_Valid 21
31	B_Valid 4	A_Valid 22	GND	A_Valid 29	GND
32	A_Valid 31	B_Valid 5	GND	A_Valid 23	A_Valid 30

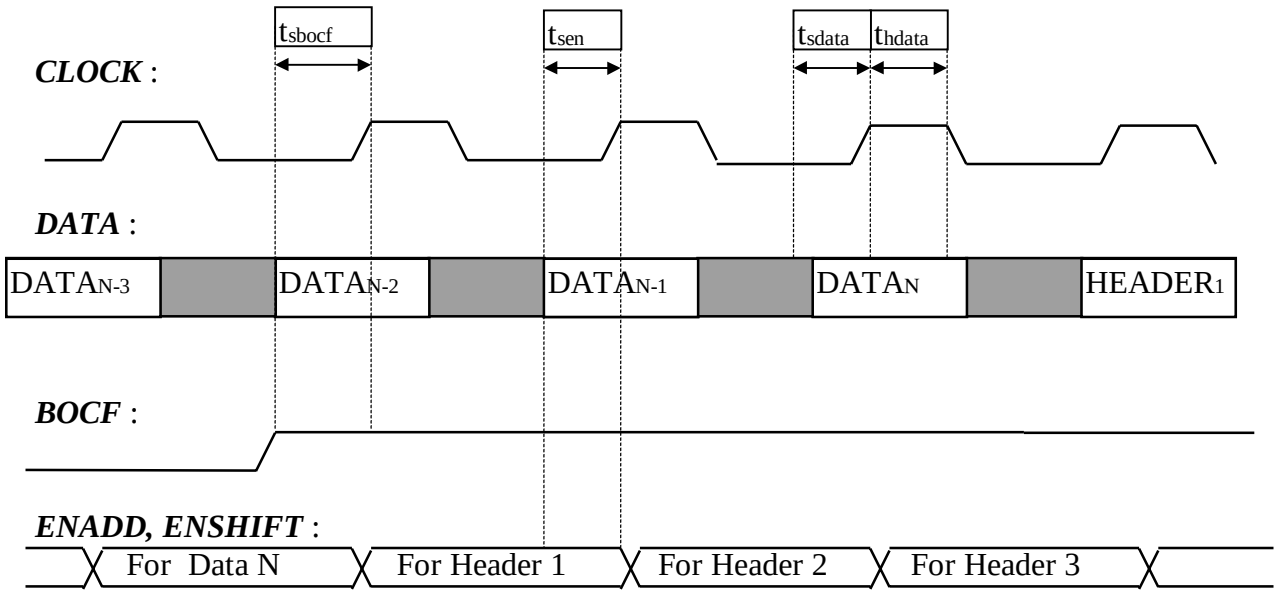
User defined pins continued :

J4	**A**	**B**	**C**	**D**	**E**
1	A_Valid 24	GND	GND	B_Valid 6	A_Valid 32
2	A_Valid 25	B_Valid 8	GND	B_Valid 7	A_Valid 26
3	B_Valid 1	GND	GND	B_Valid 9	B_Valid 19
4	B_Valid 14	B_Valid 10	GND	B_Valid 20	B_Valid 15
5	GND	B_Valid 11	GND	GND	GND
6	B_Valid 21	B_Valid 16	GND	B_Valid 12	B_Valid 22
7	B_Valid 17	B_Valid 13	GND	B_Valid 23	B_Valid 18
8	B_Valid 25	GND	GND	B_Valid 24	B_Valid 32
9	B_Valid 27	B_Valid 26	GND	B_Valid 28	B_Valid 29
10	GND	B_Valid 30	GND	GND	GND
11	B_Valid 31	A_Mag 15	GND	A_Mag 9	A_Mag 4
12	A_Mag 16	A_Mag 10	GND	A_Mag 5	A_Mag 17
13	A_Mag 11	GND	GND	A_Mag 6	A_Mag 18
14	A_Mag 12	A_Mag 7	GND	A_Mag 19	A_Mag 3
15	GND	A_Mag 13	GND	GND	GND
16	A_Mag 8	A_Mag 14	GND	A_Mag 2	A_Mag 27
17	A_Mag 1	A_Mag 20	GND	B_Mag 2	A_Mag 28
18	A_Mag 21	GND	GND	B_Mag 3	A_Mag 29
19	A_Mag 22	B_Mag 4	GND	A_Mag 30	A_Mag 23
20	GND	B_Mag 5	GND	GND	GND
21	A_Mag 31	A_Mag 24	GND	B_Mag 6	A_Mag 32
22	A_Mag 25	B_Mag 8	GND	B_Mag 7	A_Mag 26
23	B_Mag 1	GND	GND	B_Mag 9	B_Mag 19
24	B_Mag 14	B_Mag 10	GND	B_Mag 20	B_Mag 15
25	GND	B_Mag 11	GND	GND	GND
26	B_Mag 21	B_Mag 16	GND	B_Mag 12	B_Mag 22
27	B_Mag 17	B_Mag 13	GND	B_Mag 23	B_Mag 18
28	B_Mag 25	GND	GND	B_Mag 24	B_Mag 32
29	B_Mag 27	B_Mag 26	GND	B_Mag 28	B_Mag 29
30	GND	B_Mag 30	GND	GND	GND

31	B_Mag 31	Spare_A4	GND	SPARE_A5	SPARE_A6
32	GND	Spare_B1	GND	SPARE_B2	CHAS GND

3.1.2.2 Back Plane Timing

The timing relationship between Clock, Data and BOCF presented **at** the correlator board from the backplane is illustrated below ;



TIMING PARAMETER	MIN (ns)	MAX (ns)
t_{sbocf}	8	N/A
t_{hbocf} (*hold time not shown*)	6	N/A
t_{sdata}	8	N/A
t_{hdata}	8	N/A
t_{sen}	8	N/A
t_{hen} (*hold time not shown*)	6	N/A

3.2 Control and Processing

All programmable devices and memory are accessible to a VME bus master. Two TMS320C40 (C40) reside on the correlator board. The processor has access to all programmable devices and memory. The VME bus master has priority in an arbitration for memory.

3.2.1 DSP Processor Interrupts

The C40 has four external interrupts. BOCF interrupts the C40 on both the rising and falling edges. By writing to one location in Dual Port RAM, a VME Bus Master interrupts the processor. The fourth interrupt signifies diagnostics complete. Interrupts are enabled or disabled by writing to an interrupt control register on board the TMS320C40. The

communication ports have interrupts that occur on events as described in chapter 3 of the "TMS320C4X Users Guide."

3.2.2 Clocks

All synchronous devices, with the exception of VME Bus interface logic and the TMS320C40's, will use the ***data*** clock or its derivative input from the backplane coax connector. VME Bus Interface logic will use SYSCLK (16 MHz) input from pin A10 on connector P1. The clock to the C40 is an on board 40 MHz crystal oscillator.

3.2.3 Cross Point Switches and Correlator Data Interface

Ten 66x64 cross point switches reside on each correlator board. Figure 2 (redrawn from [1]) shows the cross point switch interface from back plane to each correlator ASIC input.

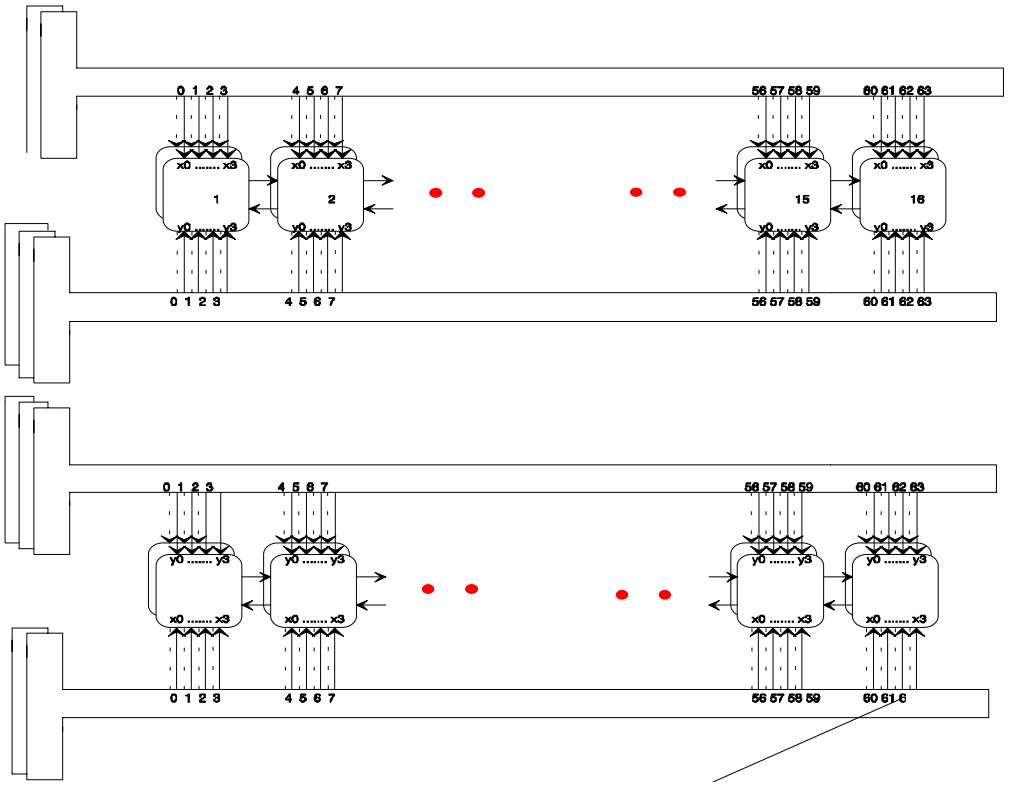


Figure 2

The 64 x 64 cross point (X Point) switches direct any of the 64 inputs to any number of the 64 output pins. Data is registered in the X point switches with respect to the *data clock*. The inputs to the XBAR may be TTL or CMOS levels, outputs into a 20 pF load are at CMOS levels.

Six of the 10 sockets reserved for X point switches are populated in VLBI applications. SMA applications require 8 X point switches.

3.2.4 DSP Correlator ASIC Interface

The two TMS320C40's on board are referred to as the Processing DSP and the I/O DSP. The C40's communicate with one another via 4 Com Ports as illustrated in Figure 1. The I/O DSP uses its local and global address and data lines to communicate with each Correlator ASIC. The I/O DSP receives commands and transfers status and data to the Processing DSP. Each Correlator ASIC holds a unique location in the Correlator Boards memory map, so that data is written or gathered one ASIC at a time. Because the local and global bus on each DSP has simultaneous access to the ASIC's, data may be gathered in parallel.

The correlator input control signals *accumulate* (ACCUM) and *shift-sample* (SHSMP) are controlled locally on the board by dividing down the clock by a specified ratio under control of a DSP-supplied parameter, with phasing being referenced to the BOCF. If necessary, the phasing of ACCUM and SHSMP with respect to BOCF can also be controlled, but it is not clear if that is necessary. Correlation Data is transfered into buffers readable by the C40 when the *load buffers* (LOADB) input control signal to the correlator is asserted. Like ACCUM and SHSMP, LOADB is locally controlled by dividing down the clock by a specified ratio under control of a DSP-supplied parameter, with phasing being referenced to the BOCF. The external signals TRDATA, ENSHIFT, ENADD, and RESET are accepted as control signals via the backplane connectors P2 and P3 when the DSP is commanded to relinquish on-board control of these signals.

Note that on board division of the clock has 5 selections, either ÷ 1, 2, 4, 8 or 16.

3.3 Memory Organization

The C40 has a *local* and *global* address and data bus with 31 address and 32 data lines. The global bus has two memory banks, each residing at a different page boundary in memory (as defined pages on 7-8 through 7-11 of the " TMS320C40 Users Guide ").

On the Processing DSP, local memory bank A and B extends to a maximum of 1M x 32 in steps of 256K x 32 when RAM is fully populated. Global memory has one bank of RAM identical in configuration to RAM bank A (or B) on the global bus. A 1K x 8 dual port RAM resides on the local bus too. One side of the Dual Port RAM is attached to the C40, the other is attached to VME Bus interface logic. The I/O DSP has 32 Kbytes of EPROM on its local bus, and 1M of RAM on its global bus.

RAM is available at speeds which will permit the processor to run without wait states. However, if less expensive "slower" RAM is used the on board logic (OBLx) will generate signals putting the C40 into a "wait state" while slower memory is accessed.

3.3.1 Processing DSP and VME Shared Memory Arbitration

The correlator arbitration logic permits both C40 and VME bus master access to RAM memory. The VME bus master is the only device that programs the arbitration logic on board, and may unilaterally choose to give RAM access to either the DSP processor or

itself. The following paragraph will illustrate one process using bilateral arbitration for memory.

Dual Port memory on the local bus permits simultaneous access by a VME bus master and the C40. Messages are passed between a VME bus master (crate controller) and the C40 without a sustained interrupt in processing. A VME bus master has the option of writing to an on board register (OBRx) which generates an interrupt to the C40. This interrupt initiates a branch to a software routine that examines messages and data written in dual port RAM by a VME bus master. Message based handshaking in an arbitration for RAM memory uses dual port RAM. The VME bus master has the option of individually selecting one RAM bank enabling the C40 to continue processing with remaining RAM.

3.3.2 Downloading Firmware

The program executed by the Processing DSP resides in RAM. At power up, onboard logic (OBLx) asserts a reset signal to bring the C40 to a known inactive state. OBLx is memory mapped onto the VME bus allowing a bus master the option of asserting or removing processor reset. The VME bus master transfers the DSP firmware into program RAM while reset is asserted. The VME bus master removes processor reset after writing firmware into program RAM. When reset is removed, the C40 begins executing intructions at a hardcoded address.

The I/O DSP has an EPROM which is used to store it's boot up procedure and optionally its software executable.

3.4 High Speed Data Interface

Control and data lines from Com Ports 0 and 5 on the C40 are available at the front panel of the correlator board through a sub-minature D connector. This will allow unloading data from memory at speeds up to 20 MBytes/sec. The Ports are unidirectional, Com Port 0 is transmit only, while Com Port 5 is receive only.

3.5 Diagnostics

Part of the design of the correlator board will facilitate automated computer controlled diagnostics capable of performing extensive operational inspection. In one mode of operation, Test RAM feeds parallel to serial shift registers (P/S), whose outputs are the inputs to the special test inputs of the XBAR switches. This allows for the cross or auto correlation of an arbitrary waveform or real VLBI data. At power up, the crate controller or the C40 has the option of starting a diagnostic mode where BOCF is generated on board, introducing data to the correlators from from P/S registers (via Test RAM). Figure 2 illustrates the block diagram hardware (logic held on ALTERA 7192 FPGA.)

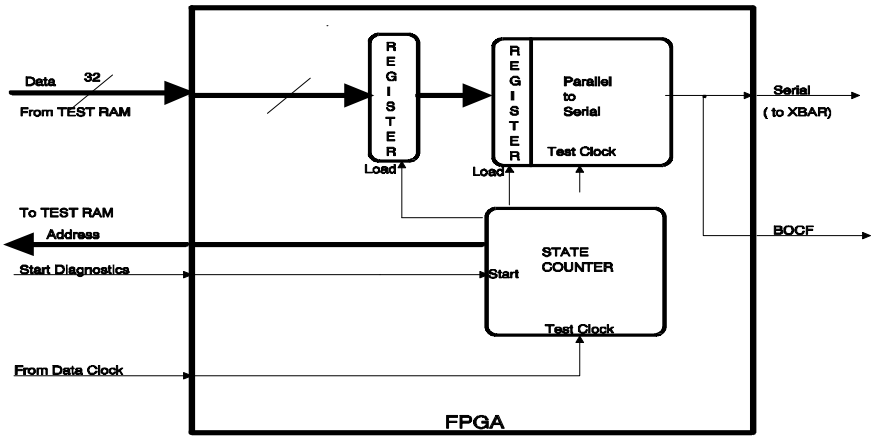


Figure 3

The crate controller has the option of putting the board into a diagnostic mode which enables the capture of data from the backplane into Test RAM. The crate controller then examines the data captured in the Test RAM insuring data is not corrupted before reaching the Correlator Board.

4.0 Software Control

The following paragraphs will define how on board logic and memory is programmed and accessed by the on board TMS320C40 ***DSP processor,*** and the ***crate controller*** via the VME bus.

4.1 VME Access

As stated in 3.1.1, the board is a VME slave residing in A32 address space. Block Transfer capability is supported. The board supports **only D32 access** and will not respond to D16 or D8 transfer requests.

The correlator board decodes VME address lines A31 through A24 in conjunction with the address modifiers to determine if the crate controller is requesting board access. The board address may be set on the correlator board via a Dip Switch (SWx).

4.1.1 VME Memory Map

The VME memory map is implemented to give the crate controller access to all devices on the correlator board. It is a superset of the TMS320C40's contiguous memory map. The VME memory map, with the exception of Local RAM A , Local RAM B and Global RAM is not contiguous due to its overlay onto C40 address space. Note that although A1 and A0 are listed in maps below, longword access requires these lines be set to logic 0 so that data is transferred on even address longword boundaries.

A23-A0	***DEVICE***
000000 - 3FFFFF	LOCAL RAM A
400000 - 7FFFFF	LOCAL RAM B
800000 - BFFFFF	GLOBAL RAM
C00000 - C1FFFF	DUAL PORT RAM
C20000 - C3FFFF	CONFIGURATION REGISTERS
C40000 - C7FFFF	CONTROL PARAMETERS
C80000 - CFFFFF	CORRELATOR GROUP A
D00000 - D7FFFF	CORRELATOR GROUP B
E00000 - EFFFFF	TEST RAM

4.1.1.1 Local RAM A, Local RAM B and Global RAM

These static RAM banks are four mega-bytes in size each. Local RAM A and B are also accessible to the C40 on its local bus, while Global RAM is accessible to the C40 on its global bus. For the Crate controller to access any RAM bank on board, the Configuration Register (4.1.1.3) must be set to award the crate controller access to that particular RAM bank while denying the C40 access.

4.1.1.2 Dual Port (DP) RAM

A23 - A16	***A15 -A12***	***A11 - A0***	***D31 - D8***	***D7 - D0***
Select DP RAM C0 - C1	X Not Used	Dual Port RAM Address	XXXXXXX Not Used	VME Data

Dual Port RAM has physical dimensions of 1K x 8. Because the board requires that all accesses be longword transfers, the virtual address space is 4K X 32. Bit's D31 through D8 do not carry valid data.

Dual Port RAM allows simultaneous access by both the C40 and Crate Controller. Arbitration logic will handle the situation of both Processors simultaneously accessing the same memory location in DP RAM memory (one processor is allowed access while the other is held in a 'wait' condition.)

The Crate Controller can interrupt the C40 by writing to one mailbox location in DP RAM. Conversely, the C40 can interrupt the crate controller by writing to one mailbox location in DP RAM.

C40				C***R***ATE CONTROLLER				
R/W1	**CE1**	**A9 - A0**	**INT1**	**R/W2**	**CE2**	**A11 - A2**	**INT2**	**FUNCTION**
L	L	3FF	X	X	X	X	L	Set INT2 Flag
X	X	X	X	X	L	3FF	H	Reset INT2 Flag
X	X	X	L	L	L	3FE	X	Set INT1 Flag
X	L	3FE	H	X	X	X	X	Reset INT1 Flag

To assert a (VME Bus) Crate Controller interrupt, the C40 writes a value into location 03FF Hex. The crate controller resets the interrupt by reading from this location. Conversely, the Crate Controller writes a value into location 03FE Hex that asserts a C40 interrupt. Note that because all interrupts are conditioned by on board logic to be edge triggered as opposed to level sensitive, continuous interrupts will not occur if the processor interrupted moves slowly in resetting the interrupt (by reading the mailbox location.) The table above is a brief synopsis of events that assert and re-arm interrupts.

4.1.1.3 Configuration Registers

A23 - A16 (Hex)	**A15 - A8 (Hex)**	**A7 - A0 (Hex)**	**Register**
C2 or C3	Don't Care	00	Local VME RAM A Enable
C2 or C3	Don't Care	04	Local VME RAM B Enable
C2 or C3	Don't Care	10	Global VME RAM Enable
C2 or C3	Don't Care	14	XBAR & ASIC Control
C2 or C3	Don't Care	18	Read Back Configuration
C2 or C3	Don't Care	20	Correlator A Access
C2 or C3	Don't Care	24	Correlator B Access
C2 or C3	Don't Care	28	IRQ Vector
C2 or C3	Don't Care	2C	IRQ Level
C2 or C3	Don't Care	30	Board ID

4.1.1.3.1 Register Definitions

Register	**Read /Write**	**D7 - D0**	**Configuration**
Local VME RAM A Enable (LVMENA)	Write	00 01	Crate Controller Has Local RAM A C40 Has Local RAM A
Local VME RAM B Enable (LVMENB)	Write	00 01	Crate Controller Has Local RAM B C40 Has Local RAM B
Global VME RAM Enable (GVMEN)	Write	00 01	Crate Controller Has Global RAM C40 Has Global RAM

XBAR and ASIC Control (XAC)	Write	01 00	C40 Access to XBAR and ASIC Control Logic Crate Controller Access to XBAR and ASIC Control Logic
Read Back Configuration	Read	nn	D0 = N/A , D1 = XAC D2 = CAA, D3 = CAB D4 = LVMENA, D5 = LVMENB D6 = GVMEN
Correlator A Access (CAA)	Write	00 01	C40 Has Correlator Group A Crate Controller Has Core Group A
Correlator B Access (CAB)	Write	00 01	C40 Has Correlator Group B Crate Controller Has Core Group B
IRQ Vector	Read/Write	nn	Sets C40 VME Interrupt Vector
IRQ Level	Read/Write	nn	Sets C40 VME Interrupt Level
Board ID	Read	nn	Board Identification

Setting the LVMENA, LVMENB and GVMEN registers govern which processor (C40 or Crate Controller) has Local RAM A, B or Global RAM access. Board Identification is set on the Correlator Board via a dipswitch and can be read electronically by the Crate Controller.

4.1.1.4 Control Parameters

A23 - A16 (Hex)	A15 - A7 (Hex)	A7 - A0 (Hex)	Register
C4 - C7	Don't Care	04	Correlator C40/Logic Reset
C4 - C7	Don't Care	08	C40 Bootup Location
C4 - C7	***nn***	0C - 30 (steps of 4)	Crossbar Chip Selects
C4 - C7	Don't Care	34	Assert Xbar Configuration
C4 - C7	Don't Care	38	Shift Sample 1 Select
C4 - C7	Don't Care	3C	Shift Sample 2 Select
C4 - C7	Don't Care	40	Sample Select
C4 - C7	Don't Care	44	Accumulate Select
C4 - C7	Don't Care	48	Diagnostic Enable
C4 - C7	Don't Care	4C	Start Diagnostic-Buffer Test
C4 - C7	Don't Care	58	Buffer Capture Enable

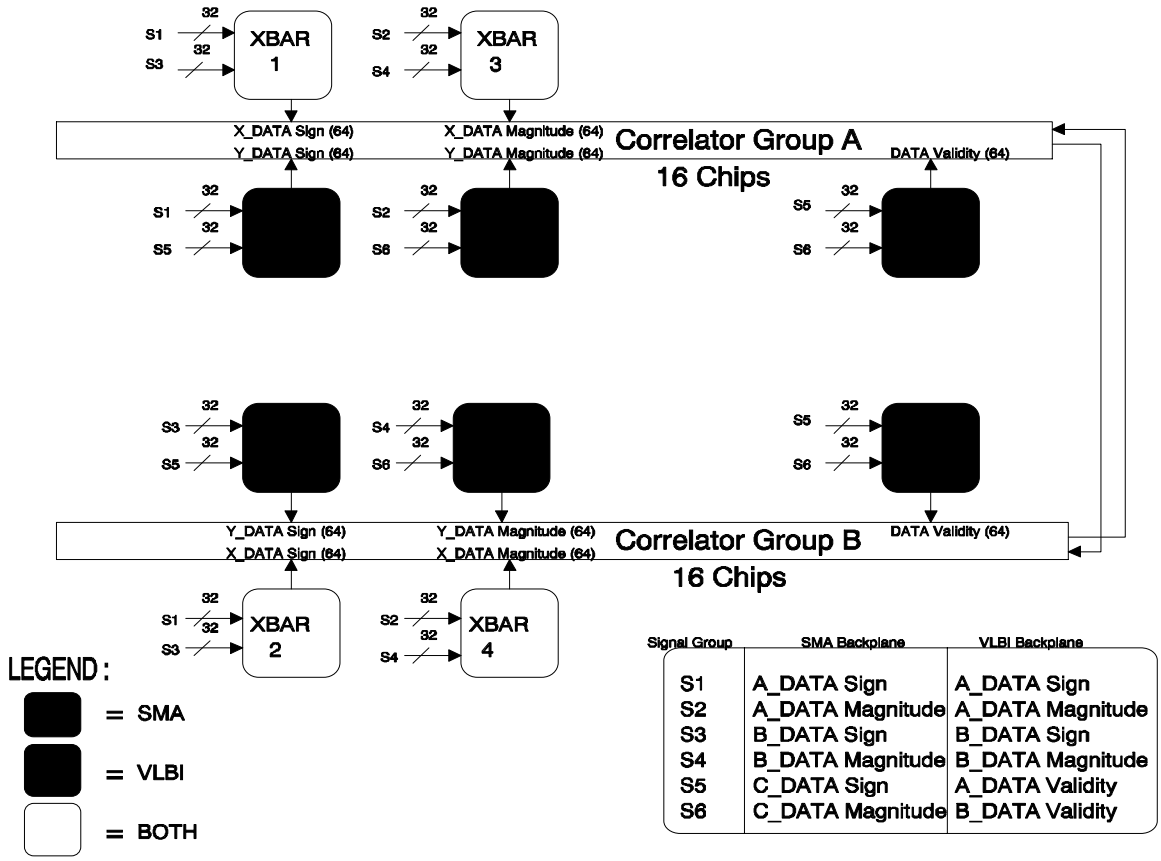
4.1.1.4.1 Register Definitions

Register	Read /Write	D15 - D0	Configuration
Correlator Logic Reset	Write	XXXn	D0 = 0 : Assert C40/Logic Reset D0 = 1 : De-assert C40/Logic Reset

C40 Bootup Location	Write	XXnn	nn = 00 : C40 Bootup Location 0 nn = 0F : C40 Bootup Location 1 nn = F0 : C40 Bootup Location 2 nn = FF : C40 Bootup Location 3
Crossbar Chip Selects	Write	Xnnn	*See 4.1.1.4.1.1*
Assert Xbar Configuration	Write	XXXX	Global XBAR Configuration
Shift Sample 1 Select	Read/Write	XXXn	BOCF inactive Shsmp Divide Rate
Shift Sample 2 Select	Read/Write	XXXn	BOCF active Shsmp Divide Rate
Sample Select	Read/Write	XXXn	Backplane or Board Corre. Control
Accumulate Select	Read/Write	XXXn	Accumulate Divide Rate
Diagnostic Enable	Write	XXXn	n = 0 : Assert Correlation Diagnostic Mode and use On Board BOCF n = 1 : Deassert Correlation Diagnostic and use Backplane BOCF
Buffer Enable	Write	XXXn	n = 0 : Assert Buffer Capture Mode n = 1 : Deassert Buffer Capture Mode
Start Diagnostic-Buffer Test	Write	XXXX	Writing to this Register Starts a Test

4.1.1.4.1.1 Xbar Configuration

The diagram below illustrates how data is distributed from the backplane, through each XBAR to the correlators. The XBAR switches have 64 on chip registers, corresponding to each output. It is possible to connect any input to any output. The XBAR switches also have two TEST inputs, to be discussed in the diagnostic section (4.1.1.7) of this document. Each output may be individually tristated. The on board XBAR control parameters are doubled buffered, allowing the host processor to configure the first set of buffers while the XBAR device continues to operate with configuration parameter's resident in the second set of buffers. When the host processor writes to the *Assert Xbar Configuration* register, data from the first set of buffers in **all** XBAR switches is transferred to the second set of buffers . On board logic will synchronize with Data Clock the transfer of data from the first set of buffers to the second. The transfer requires only one Data Clock cycle before the XBAR switch can resume operation with the new configuration data. Note that in the examples below, inputs range in number from 0 to 63, as do outputs.



A5	**A4**	**A3**	**A2**	**XBAR n**
0	0	1	1	XBAR 1
0	1	0	0	XBAR 2
0	1	0	1	XBAR 3
:	:	:	:	:
1	1	0	0	XBAR 10

Address lines **A15 - A10** select 1 of 64 Output Configuration Registers (OCF) on board the XBAR switch . For example, **A15 - A10** = 0 points to OCF 0, **A15 -A10** = 1 points to OCF 1, **A15 - A10** = 3F points to OCF 63.

DATA LINES **D5 - D0**	These data lines determine which input is connected to a particular output. For example, when D5 - D0 = 9, Input 9 is connected to the Output Selected.
DATA LINE **D6**	Selects one of the two TEST inputs for the selected output. D6 = 0 (TEST 0 Select), D6 = 1 (TEST 1 Select).
DATA LINE **D7**	Enables Output to receive one of two TEST inputs when set to a logic 1.

Example : It's desired to connect input 3 to output 20 on XBAR switch 5.

Address line A23 - A0 = C4501C (Hex).
Data lines D7 - D0 = 03 (Hex).

4.1.1.4.1.2 Sample, Shift and Accumulate Select

The correlator ASIC control signals Shift Sample (SHSMP) and Accumulate (ACCUM) are generated by on board logic. Each signal may be divided down by either 0 (always active), 2 4 8, or 16 with respect to the data clock and are phase referenced to the rising edge of BOCF. SHSMP may have two different division values, one for BOCF active and one for BOCF inactive. This provision insures that if data is being sampled by some multiple of the data clock, header data that is captured during BOCF active is sampled properly. If the on board logic is directed to ignore BOCF, data is correlated during BOCF active. The correlator control signals ENSHIFT (same as SHSMP), ENADD (same as ACCUM), TRDATA and CLEAR are available on backplane connector pins from J3 and J4. On board logic generating these signals can be switched off, enabling the backplane signals listed above to directly control these correlator ASIC functions. These signals are not conditioned (i.e. divided down) by on board logic.

Signal	**D7 .. D0**	**Effect**
SHSMP 1 Select SMSMP 2 Select and ACCUM	00000000 00000001 00000010 00000011 000001XX 00001XXX NNNNXXXX	Divide By 2 Divide By 4 Divide By 8 Divide By 16 Always Active Always Inactive On READ, NNNN = Count - 2 of clocks before BOCF rising edge
Sample Select	0000001X 000000X1 00000000 NNNNXXXX	Ignore BOCF Use Backplane Correlator Control Signals ENADD, ENSHIFT, TRDATA and CLEAR Pay attention to BOCF, use on board Correlator Control Signals (Standard Operation) On READ, NNNN = Count - 2 of clocks before BOCF rising edge

4.1.1.5 Correlator Group A

The specific correlator ASIC control signals are as follows :

Control Signal	**A18 - A14**	**A13 - A10**	**Effect (Group A)**
Chip Enable	XXXXX	0000 0001 : 1111	Select Correlator Chip 1 Select Correlator Chip 2 : Select Correlator Chip 16
Initialize State	00001	XXXX	Initialize Dynamic Parameter State Machine
Select Lag	00010	XXXX	Select Lags (Read Only)
Select DP	00011	XXXX	Select Dynamic Parameters
Select SP	00100	XXXX	Select Static Parameters
Test	00101	XXXX	D30 = 0 : Test is set at a Logic Low D30 = 1 : Test is set at a Logic High

Valctr	00110	XXXX	D30 = 0 : Validity Counter is set Logic Low D30 = 1 : Validity Counter is set Logic High
ClearSP	00111	XXXX	Clear Static Parameters
Initsr	01000	XXXX	Initialialize Registers

Chip Enable is used in conjunction with the other correlator control signals. For example, if it is desired to read lags on Correlator Chip 6, A18 - A10 is set to 00010 0110 (Binary) .

The effect these signals have on Correlator ASIC operation is defined in [2].

4.1.1.6 Correlator Group B

The specific correlator ASIC control signals are as follows :

Control Signal	**A18 - A14**	**A13 - A10**	**Effect (Group B)**
Chip Enable	XXXXX	0000 0001 : 1111	Select Correlator Chip 17 Select Correlator Chip 18 : Select Correlator Chip 32
Initialize State	00001	XXXX	Initialize Dynamic Parameter State Machine
Select Lag	00010	XXXX	Select Lags (Read Only)
Select DP	00011	XXXX	Select Dynamic Parameters
Select SP	00100	XXXX	Select Static Parameters
Test	00101	XXXX	D30 = 0 : Test is set at a Logic Low D30 = 1 : Test is set at a Logic High
Valctr	00110	XXXX	D30 = 0 : Validity Counter is set Logic Low D30 = 1 : Validity Counter is set Logic High
ClearSP	00111	XXXX	Clear Static Parameters
Initsr	01000	XXXX	Initialialize Registers

Chip Enable is used in conjunction with the other correlator control signals. For example, if it is desired to read lags on Correlator Chip22, A18 - A10 is set to 00010 0110 (Binary). The effect these signals have on Correlator ASIC operation is defined in [2].

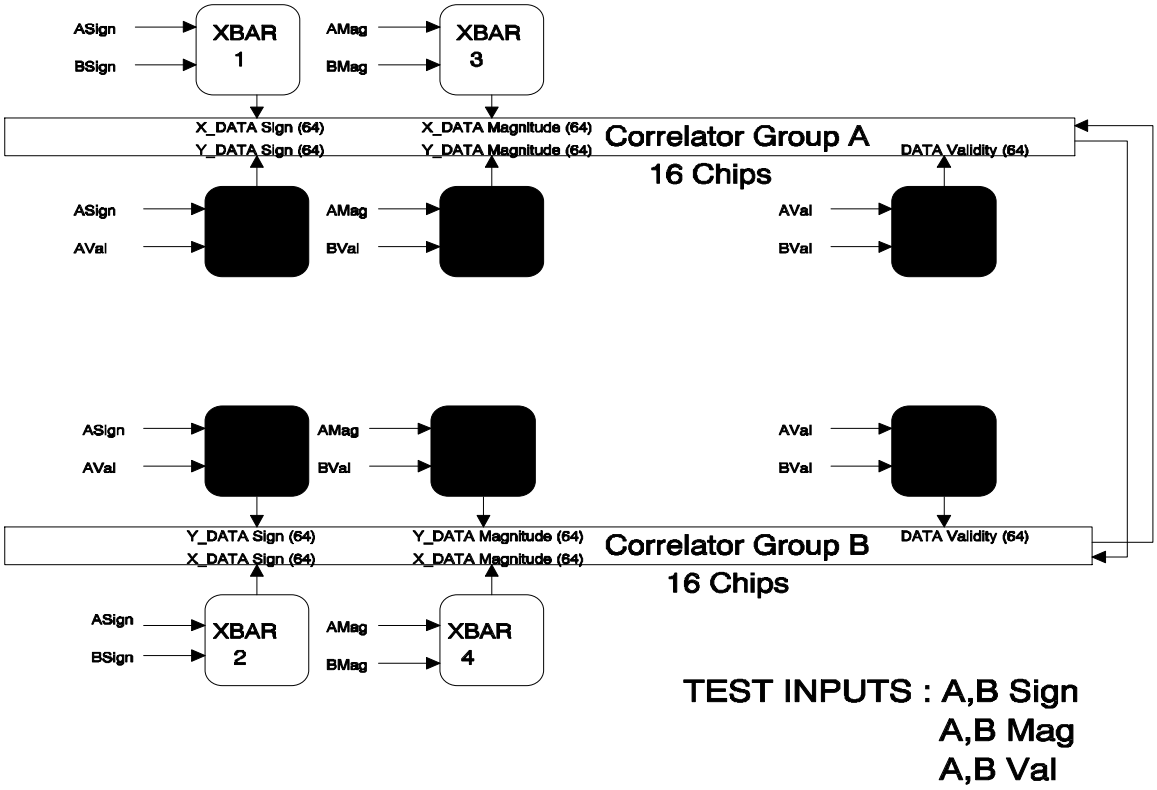
4.1.1.7 Diagnostics

The correlator board has hardware provisions for a comprehensive cross or auto correlation test. On board is a special 256K x 32 RAM (*Test RAM*) accessible to the crate controller only. The data lines of this RAM feed both VME and a FPGA configured to serialize and direct the data to special test inputs on the XBAR switches. The correlator board can be placed in a mode where data from the backplane is packeted by an FPGA and written to Test RAM (data buffer capture).

4.1.1.7.1 Correlation Test

The XBAR switches have 66 inputs, 64 of which are connected to backplane signal inputs, while the other two *test* inputs are connected to the output of an FPGA. This same FPGA accepts 32 bit data in Parallel from the Test RAM and converts it to a serial data stream output destined for the *test* input of the XBAR switches.

The following diagram details the location of test inputs into the XBAR switches ;



The organization of *data* in test RAM is as follows :

D0	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
ASign	AMag	AVal	BSign	BMag	BVal	BOCF	DONE
D8	**D9**	**D10**	**D11**	**D12**	**D13**	**D14**	**D15**
ASign	AMag	AVal	BSign	BMag	BVal	BOCF	DONE
D16	**D17**	**D18**	**D19**	**D20**	**D21**	**D22**	**D23**
ASign	AMag	AVal	BSign	BMag	BVal	BOCF	DONE
D24	**D25**	**D26**	**D27**	**D28**	**D29**	**D30**	**D31**
ASign	AMag	AVal	BSign	BMag	BVal	BOCF	DONE

Data is organized in longword format. Each row of data is presented to the XBAR switches at the beginning of a clock cycle. Test Done is set to logic 0 for diagnostic operation and logic 1 to terminate the diganostic test. The test will automatically terminate

if TDONE is not set when the maximum count of 256K (Test RAM is 256K x 32) is reached.

Starting a diagnostic test entails configuring the XBAR switches, enabling *Diagnostic Mode, Starting Diagnostics (**4.1.1.4**)*, and reading back resultant lags from the correlator ASIC's after the test is complete. Note that although BOCF is generated on board, Data Clock is **not**, requiring that Data Clock be present on the backplane for this test to take place.

4.1.1.7.2 Buffer Capture

In the diagnostic mode "Buffer Capture", three data streams from XBAR's 1, 3 and 9 (as shown in the previous diagram) corresponding to one bit of Sign, Magnitude and Validity is captured in Test RAM. Output_0 and Output_1 on each of the XBAR's will feed a FPGA, which will pack eight 3 bit values into one 32 bit word, then write this value to RAM. Data is captured in Test RAM after enabling *Buffer Capture Diagnostic Mode*, and then issuing a *Start Test* (4.1.1.4.1) command. Data is packed in RAM as follows ;

D0	**D1**	**D2**	**D3**	**D4**	**D5**	**D6**	**D7**
ASign	AMag	AVal	BSign	BMag	BVal	BOCF	N/A
D8	**D9**	**D10**	**D11**	**D12**	**D13**	**D14**	**D15**
ASign	AMag	AVal	BSign	BMag	BVal	BOCF	N/A
D16	**D17**	**D18**	**D19**	**D20**	**D21**	**D22**	**D23**
ASign	AMag	AVal	BSign	BMag	BVal	BOCF	N/A
D24	**D25**	**D26**	**D27**	**D28**	**D29**	**D30**	**D31**
ASign	AMag	AVal	BSign	BMag	BVal	BOCF	N/A

Data is captured starting at address 0. The first valid sample is captured on the rising edge of BOCF, and subsequent samples fill Test RAM (256K x 32) to its full capacity.

4.2 On Board Processing and I/O (TMS320C40's)

On the correlator board will reside two DSP processors that have different I/O and processing responsibilities. Although there is flexibility in assigning tasks to each DSP, their intent and designation are as follows; The *processing DSP* as depicted in Figure 1 is used for storage and data retrieval, as well as computational intensive tasks on the data. The predominant amount of RAM memory is attached to this processor. The processing DSP also has a *Dual Port Ram* attached to it enabling two way communication with the Crate Controller. In a sense this DSP may be thought of as on board command and control, which executes tasks issued by the Crate Controller and sends back status.

The *I/O DSP* as depicted in Figure 1 has the primary responsibility to interface with the Correlator ASIC's. It gathers data from the ASIC's during a correlator frame and passes this information on (via Com Ports) to the processing DSP. The I/O DSP has EPROM for program storage, as well as RAM for optional processing capability.

The Processing DSP has only volatile memory (RAM) attached to it, therefore its executable program has to be downloaded by the Crate Controller (CC). The sequence of events that occur are; The CC puts the C40 in a reset state and sets the "Boot up Location." It then transfers the program down into RAM, then removes reset so that the C40 begins execution at the boot up location. Because the I/O DSP has non-volatile memory (EPROM), it's executable starts at the fixed boot up location 0000 0000 (hex) in EPROM.

The I/O DSP and Processing DSP communicate with one another via Com Ports. This document does not to describe the Com Ports function in detail, however the interested reader will find Chapters 8 and 9 in the 1991 edition of the TMS320C40 Users Guide useful. Com Port interconnect between the two DSP's and external interfaces is as follows;

I/O DSP Com Port	**Processing DSP Com Port**	**Comment**
Com Port 0 ***to***	Com Port 3	
Com Port 1 ***to***	Com Port 4	
Com Port 3 ***to***	Com Port 1	
Com Port 4 ***to***	Com Port 2	
N/A	Com Ports 0, 5 ***to***	External Connector

Com Ports 0,5 provide a means other than the VME bus for transferring data. Com Port 0 is used to send data (alway's transmit), while Com Port 5 is used to receive data (alway's receive). Com Ports 0 and 5 on the Processing DSP are **not** designed to be bidirectional, but instead are unidirectional. The front panel connector used for carrying Com Port's signals is a 48 pin DIN style connector. The pin out is as follows;

A1	C0D0	**B1**	GND	**C1**	C5D0
A2	C0D1	**B2**	GND	**C2**	C5D1
A3	C0D2	**B3**	GND	**C3**	C5D2
A4	C0D3	**B4**	GND	**C4**	C5D3
A5	GND	**B5**	GND	**C5**	GND
A6	C0D4	**B6**	GND	**C6**	C5D4
A7	C0D5	**B7**	GND	**C7**	C5D5
A8	C0D6	**B8**	GND	**C8**	C5D6
A9	C0D7	**B9**	GND	**C9**	C5D7
A10	GND	**B10**	GND	**C10**	GND
A11	CREQ0	**B11**	GND	**C11**	CREQ5
A12	CACK0	**B12**	GND	**C12**	CACK5
A13	GND	**B13**	GND	**C13**	GND
A14	CSTRB0	**B14**	GND	**C14**	CSTRB5
A15	GND	**B15**	GND	**C15**	GND
A16	CREADY0	**B16**	GND	**C16**	CREADY5

4.2.1 Processing DSP Memory Map

The Processing DSP's external memory map is a subset of the VME memory map. There is an address offset difference between VME and DSP memory map, therefore DSP memory and logic addresses are explicitly stated. For a detailed description of functions, please refer to section ***4.1 VME Access*** and the significant subsections under this heading. Internal memory map detailed descriptions are available in the 1991 edition of the TMS320C40 Users Guide.

A31 - A0	***DEVICE***
0000 0000 - 000F FFFF	LOCAL RAM A
0010 0000 - 002F FFFF	INTERNAL MEMORY AND CONTROL
00C0 0000 - 00CF FFFF	LOCAL RAM B
8000 0000 - 800F FFFF	GLOBAL RAM
8010 0000 - 801F FFFF	CONTROL PARAMETERS
8020 0000 - 8020 03FF	DUAL PORT RAM

Local RAM A and B respond to LSTRB0, Global RAM and Control Parameters to STRB0, and Dual Port RAM to STRB1. (L)STRB signals are defined in the TMS320C40 Users Guide.

4.2.1.1 Internal Memory and Control

This information can be found in the TMS320C40 Users Guide.

4.2.1.2 Control Parameters

A15 - A0 {A31 - A16 = 8010}	**Register**
0003 - 000C	XBAR Chip Select 1 - 10
000D	Assert XBAR Configuration
000E	Shift Sample 1 Select
000F	Shift Sample 2 Select
0010	Sample Select
0011	Accumulate Select
0012	Diagnostic Enable
0013	Start Diagnostic Buffer Test
0014	Error Indicator {D0 = Dessert, =1 Assert}
0016	Buffer Capture Enable

4.2.1.3 Dual Port RAM

Mailbox interrupts are described in section ***4.1.1.2 DP RAM*** in under ***VME Access***.

4.2.2 I/O DSP Memory Map

Program execution starts in EPROM at address 0000 0000 (hex). A 1 Mbyte RAM module {optional} is attached to the global bus. Unlike all other RAM modules on the board, this RAM module is not directly accessible to the Crate Controller via the VME bus.

A31 - A0	***DEVICE***
0000 0000 - 0000 1FFF	EPROM
0002 0000 - 0002 8FFF	CORRELATOR GROUP A
0010 0000 - 002F FFFF	INTERNAL MEMORY AND CONTROL
8000 0000 - 8003 FFFF	I/O RAM
8004 0000 - 8004 8FFF	CORRELATOR GROUP B

EPROM responds to LSTRB0, Correlator Group A to LSTRB1. I/O RAM responds to STRB0, Correlator Group B to STRB1. (L)STRB signals are defined in the TMS320C40 Users Guide.

4.2.2.1 Correlator Group A

Address A31 - A16 = 0002 (hex), and the specific correlator ASIC control signals are as follows (in binary):

Control Signal	**A15 - A12**	**A11 - A8**	**Effect (Group A)**
Chip Enable	XXXX	0000 0001 : 1111	Select Correlator Chip 1 Select Correlator Chip 2 : Select Correlator Chip 16
Initialize State	0001	XXXX	Initialize Dynamic Parameter State Machine
Select Lag	0010	XXXX	Select Lags (Read Only)
Select DP	0011	XXXX	Select Dynamic Parameters
Select SP	0100	XXXX	Select Static Parameters
Test	0101	XXXX	D30 = 0 : Test is set at a Logic Low D30 = 1 : Test is set at a Logic High
Valctr	0110	XXXX	D30 = 0 : Validity Counter is set Logic Low D30 = 1 : Validity Counter is set Logic High
ClearSP	0111	XXXX	Clear Static Parameters
Initsr	1000	XXXX	Initialialize Registers

Chip Enable is used in conjunction with the other correlator control signals. For example, if it is desired to read lags on Correlator Chip 6, A15 - A8 is set to 0010 0110 (Binary) .

The effect these signals have on Correlator ASIC operation is defined in [2].

4.2.2.2 Correlator Group B

Address A31 - A16 = 8004 (hex), and the specific correlator ASIC control signals are as follows (in binary):

Control Signal	A15 - A12	A11 - A8	Effect (Group B)
Chip Enable	XXXX	0000 0001 : 1111	Select Correlator Chip 17 Select Correlator Chip 18 : Select Correlator Chip 32
Initialize State	0001	XXXX	Initialize Dynamic Parameter State Machine
Select Lag	0010	XXXX	Select Lags (Read Only)
Select DP	0011	XXXX	Select Dynamic Parameters
Select SP	0100	XXXX	Select Static Parameters
Test	0101	XXXX	D30 = 0 : Test is set at a Logic Low D30 = 1 : Test is set at a Logic High
Valctr	0110	XXXX	D30 = 0 : Validity Counter is set Logic Low D30 = 1 : Validity Counter is set Logic High
ClearSP	0111	XXXX	Clear Static Parameters
Initsr	1000	XXXX	Initialialize Registers

Chip Enable is used in conjunction with the other correlator control signals. For example, if it is desired to read lags on Correlator Chip22, A15 - A8 is set to 0010 0110 (Binary).

The effect these signals have on Correlator ASIC operation is defined in [2].

5.0 Mechanical Considerations and Power Requirements

(TO BE COMPLETED)