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To: Mark IV Development Group

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Subject: Serial Link Interface Specification

The G-Link Transmitter and Receiver Modules are general-purpose data link modules and can be used in a multitude of data-transmission applications from 4.5 MHz to 60 MHz. The Advanced VLBI and WSRT Correlators require three kinds of links:

- Single multiplexed 25-bit links at 32 or 40 MHz for use with a data distributor.
- Dual 13-bit links at 32 MHz for the DDU-less Mark IV Correlator, which requires four data links from each SU, one to each Correlator Input Board. (See Mark IV Memos #194 and #197.)
- Single 20-bit links at 5, 10, or 32 MHz for distribution of system synchronization, test, and pulsar gate signals.

1. Pin Assignments are shown in the tables on the following pages.

2. Mechanical

   A sketch showing placement of components for a multiplexed single-link module is attached.

   Board Size: 60x114 mm
   Robinson Nugent connector types:
   Link board: P50L-050P-A-TGF Plug
   Mother board: P50L-050S-x-TGF Socket
   See RN catalog for Pin Out Identification.
   Connector locations: 104.1 mm apart
   Coaxial connectors: SMC (SMA optional)

NOTE: This memo is a revision of Mark IV Memo #198.1 dated 22 September 1994.

3. Electrical

RESET* (Chip Power-up Reset, active low)

Transmitter Status Signal:
READY (Ready for Data, Transmitter is locked to DCLOCK)

Receiver Control and Status Signals:
READY (STAT0, Receiver is locked to DIN)
XCLOCK (Reference clock to LIN for simplex synchronization)
ERROR

There will be jumpers on the single-link modules to configure the following link parameters:
FLAGSEL
M20SEL
DIV0
DIV1
EQEN

Power Requirements:

VCC	+5V ±5%	1000	mA
VEE	5V ±10%	1300	mA (Dual link)
		860	mA (Multiplexed link)

4. See other relevant documents:
Hewlett Packard HDMP-1012/14 Serial Link Data Sheet
Motorola MC100H600/601 TTL/ECL/TTL Translator Data Sheets
Cypress CY7B991 Clock Buffer Data Sheet
Xilinx Programmable Logic Data Book

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SYSTEM DATA INTERFACES
PIN ASSIGNMENTS
TRANSMITTER LINK:

SU INTERFACE MODULE, DD POST-SELECTOR BOARD

J1:	A:	B:	J2:	A:	B:
1	GND	TS	1	ECLGND	VEE
2	GND	TM	2	ECLGND	VEE
3	GND	TV	3	GND	~TEST
4	GND	S0	4	GND	S4
5	GND	S1	5	GND	S5
6	GND	S2	6	GND	S6
7	GND	S3	7	GND	S7
8	GND	M0	8	GND	M4
9	GND	M1	9	GND	M5
10	GND	M2	10	GND	M6
11	GND	M3	11	GND	M7
12	ECLGND	VEE	12	GND	VCC
13	ECLGND	VEE	13	GND	VCC
14	ECLGND	VEE	14	GND	VCC
15	GND	V0	15	GND	V4
16	GND	V1	16	GND	V5
17	GND	V2	17	GND	V6
18	GND	V3	18	GND	V7
19	GND	BOCF	19	GND	TSO
20	GND	DCLOCK	20	GND	TMO
21	GND	RANDOM	21	GND	TVO
22	GND	~DAV	22	GND	DCLOCK
23	ECLGND	READY0	23	GND	~DAV
24	GND	CLTEST	24	ECLGND	READY1
25	GND	STMODE	25	GND	~RESET

SYSREF (5/10 MHz), TSPU (32 MHz)

J1:	A:	B:	J2:	A:	B:
1	GND	GND	1	ECLGND	VEE
2	GND	GND	2	ECLGND	VEE
3	GND	GND	3	GND	GND
4	GND	D0	4	GND	D12
5	GND	D1	5	GND	D13
6	GND	D2	6	GND	D14
7	GND	D3	7	GND	D15
8	GND	D4	8	GND	D16
9	GND	D5	9	GND	D17
10	GND	D6	10	GND	D18
11	GND	D7	11	GND	D19
12	ECLGND	VEE	12	GND	VCC
13	ECLGND	VEE	13	GND	VCC
14	ECLGND	VEE	14	GND	VCC
15	GND	D8	15	GND	GND
16	GND	D9	16	GND	GND
17	GND	D10	17	GND	GND
18	GND	D11	18	GND	GND
19	GND	FLAG	19	GND	N/C
20	GND	DCLOCK	20	GND	N/C
21	GND	GND	21	GND	N/C
22	GND	~DAV	22	GND	DCLOCK
23	ECLGND	READY	23	GND	~DAV
24	GND	GND	24	ECLGND	READY
25	GND	GND	25	GND	~RESET

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SYSTEM DATA INTERFACES
PIN ASSIGNMENTS
RECEIVER LINK:

DD PRE-SELECTOR BOARD, CORRELATOR INPUT BOARD

J1:	A:	B:	J2:	A:	B:
1	GND	TS	1	ECLGND	VEE
2	GND	TM	2	ECLGND	VEE
3	GND	TV	3	CLEAR	~TEST
4	GND	S0	4	GND	S4
5	GND	S1	5	GND	S5
6	GND	S2	6	GND	S6
7	GND	S3	7	GND	S7
8	GND	M0	8	GND	M4
9	GND	M1	9	GND	M5
10	GND	M2	10	GND	M6
11	GND	M3	11	GND	M7
12	ECLGND	VEE	12	GND	VCC
13	ECLGND	VEE	13	GND	VCC
14	ECLGND	VEE	14	GND	VCC
15	GND	V0	15	GND	V4
16	GND	V1	16	GND	V5
17	GND	V2	17	GND	V6
18	GND	V3	18	GND	V7
19	GND	BOCF0	19	GND	BOCF1
20	GND	DCLOCK0	20	GND	DCLOCK1
21	GND	ERROR0	21	GND	ERROR1
22	GND	~DAV0	22	GND	~DAV1
23	GND	READY0	23	GND	READY1
24	ECLGND	XCLOCK0	24	GND	TCLOCK
25	ECLGND	~RESET	25	ECLGND	XCLOCK1

TSPU (5/10 MHz), SUIM (32 MHz)

J1:	A:	B:	J2:	A:	B:
1	GND	GND	1	ECLGND	VEE
2	GND	GND	2	ECLGND	VEE
3	GND	GND	3	GND	GND
4	GND	D0	4	GND	D12
5	GND	D1	5	GND	D13
6	GND	D2	6	GND	D14
7	GND	D3	7	GND	D15
8	GND	D4	8	GND	D16
9	GND	D5	9	GND	D17
10	GND	D6	10	GND	D18
11	GND	D7	11	GND	D19
12	ECLGND	VEE	12	GND	VCC
13	ECLGND	VEE	13	GND	VCC
14	ECLGND	VEE	14	GND	VCC
15	GND	D8	15	GND	D8
16	GND	D9	16	GND	D9
17	GND	D10	17	GND	D10
18	GND	D11	18	GND	D11
19	GND	FLAG	19	GND	FLAG
20	GND	DCLOCK	20	GND	DCLOCK
21	GND	ERROR	21	GND	ERROR
22	GND	~DAV	22	GND	~DAV
23	GND	READY	23	GND	READY
24	ECLGND	XCLOCK	24	GND	GND
25	ECLGND	~RESET	25	ECLGND	unused

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TRANSMITTER LINK
INPUT SIGNALS:

DATA	TTL	10 uA	10 pF to XC73108 or MC100H600
BOCF	TTL	10 uA	10 pF
FLAG	TTL	10 uA	10 pF
~TEST	TTL	10 uA	10 pF
RANDOM	TTL	10 uA	10 pF
CLTEST	TTL	10 uA	10 pF (test clock @ 0.5/0.625 MHz)
~RESET	TTL	-0.6 mA	10 pF to MC100H600
~DAV	TTL	-0.6 mA	10 pF to MC100H600
DCLOCK	TTL	10 uA	10 pF to XC73108 for multiplexed link
	1.0 to 5V peak-to-peak into 250 Ω for direct link, ac coupled		

OUTPUT SIGNALS:

TS,TMO,TVO	TTL	-4 mA	35 pF from XC73108
READY0-1	ECL	300 ohm	from HDMP-1012
DOUT	600mV peak-to-peak into 50 Ω, ac coupled, from HDMP-1012		

RECEIVER LINK
OUTPUT SIGNALS:

DATA	TTL	-4 mA	35 pF from XC7336 or MC100H600
BOCF0-1	TTL	-4 mA	35 pF
DCLOCK0-1	TTL	-15 mA	50 pF from CY7B991 or MC100H600
~DAV0-1	TTL	-15 mA	50 pF from MC100H600
READY0-1	TTL	-15 mA	50 pF
ERROR0-1	TTL	-15 mA	50 pF

INPUT SIGNALS:

DIN	0.2 to 2V peak-to-peak into 50 Ω, ac coupled to HDMP-1014
XCLOCK	1.0 to 5V peak-to-peak into 250 Ω, ac coupled to HDMP-1014 f=32 MHz(Mk4),48 MHz(EVN),60 MHz(DZB) XCLOCK is ac coupled to a 250-ohm load, and can be driven by a TTL or CMOS clock driver.

TS,TM,TV	TTL	10 uA	10 pF to XC7336
~TEST	TTL	40 uA	40 pF to four XC7336s
TCLOCK	TTL	10 uA	10 pF to XC7336 (test clock @ 16/20 MHz)
~RESET	ECL	300 ohm to HDMP-1014	

POWER:

VCC	+5V +/-5%	1000 mA
VEE	-5V+/-10%	1300 mA (Dual link)
(Multiplexed link:		860 mA)

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