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To: Mark IV Development Group

From: Dan L. Smythe

Subject: SYSTICK Generator

To provide CLREF and SYSTICK to the Correlator Control Board for test purposes, I have programmed one of the EPLDs on a Single Receiver Data Link board to provide 5 MHz and 1 PPS to the Control Board. A schematic diagram of the modified prototype (DEC 94) Single Rx board and the EPLD are attached. The pin assignments on the 5-MHz oscillator should work with almost any 8- or 14-pin TTL oscillator. The symbol CD3RE in the Systick Generator is a quinary counter of my own design. It could be replaced with a decade counter for use with a 10-MHz CLREF oscillator. A Single Tx board could be modified in a similar way to provide synchronized CLREF and SYSTICK signals to multiple Control Boards and to a TSPU.