

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS 01886

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Telephone: 508-692-4764

Fax: 617-981-0590

To: Mark IV Development Group

From: Dan L. Smythe

Subject: System Sync Generator

I have re-programmed the EPLD on a Single Transmitter Data Link board to provide 10 MHz and 1 PPS over a Direct Link to the Control Board, and BOCF to a Single or Dual Transmitter Data Link. This System Sync Module can be used with a Transmitter Link to provide CLREF and SYSTICK to the Control Board, with synchronized test signals to the Input Board over Serial Data Links. The 10 MHz reference is derived from the 32 MHz clock using the PLL in the Cypress Clock Buffer, which will not run below 9 MHz. Schematic diagrams of the unmodified Single Tx board and the EPLD are attached. A Data Link Test Fixture board has been modified to provide the 32 MHz to the Sync Generator Module, and BOCF from this module to the Transmitter Module. This Sync Generator has been tested from 29 MHz up to 60 MHz using an XC73108-12WC44; so it should work to at least 36 MHz using an XC7372-20WC44. Computer simulations show the '7372-20 working up to 52 MHz. This same Sync Module can be used with a microwave power divider to provide sync signals to the TSPU and Control Boards in a complete correlator system. The system clock frequency would be controlled by a 32-MHz TTL clock chip, easily changed to some other frequency above 29 MHz if desired.