MASSACHUSETTS INSTITUTE OF TECHNOLOGY
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS 01886

27 March, 1998

Telephone: 508-692-4764
Fax: 617-981-0590

To: Mark4 Recording Development Group

From: Joel I. Goodman and Hans F. Hinteregger

Re: Timing recovery and gain control for proposed DSP read channel

RELATED DOCUMENTS

[1] "A DSP read channel for increased linear density in VLBI tape recording," J.I. Goodman, H.F. Hinteregger, 21 March, 1997, Mark4 Memo # 247

INTRODUCTION

In conjunction with the DSP hardware used to adaptively and optimally decode data from tape at increased linear densities as outlined in [1], there is a need to include a way of recovering a clock from the data, removing any DC content'and baseline wander, and accounting for variations in signal amplitude. The discussion section of this document describes the theory and architecture of the hardware that will carry out these tasks. All the approaches outlined below are digital in nature, and will first be simulated in software to test their operational effectiveness.

DISCUSSION

Timing Recovery

Timing recovery is the process of recovering a synchronous clock used to write data values on tape from samples received during playback. A *maximum likelihood* approach to recover the clock is to minimize the mean square error (MSE) between the samples at the output of FIR adaptive equalizer and the chosen candidate sample of the sequence detector. The output of the equalizer described as

$$y(m,\tau) = \sum_{n} h(n)x(mT - nT - \tau) + v(mT)$$

has MSE

$$MSE = E\{[d(m) - y(m,\tau)]^2\}$$

where d(m) is the output of the sequence detector, y(m) is the input to the sequence detector, x(m) is the output of the analog to digital converter, h(n) are the FIR tap coefficients, and τ is the timing or clock phase. Minimizing the MSE by differentiating with respect to τ and setting the equation above to zero yields

$$\sum_m \{d(m) - y(m,\tau)\} y'(m,\tau) = 0$$

An interpretation of the equation above is that the optimum sampling time corresponds to the condition that the error signal [d(m) - y(m, τ)] is uncorrelated with the derivative. Since the detector output is used in the formation of the error signal, timing phase estimation is *decision directed*.

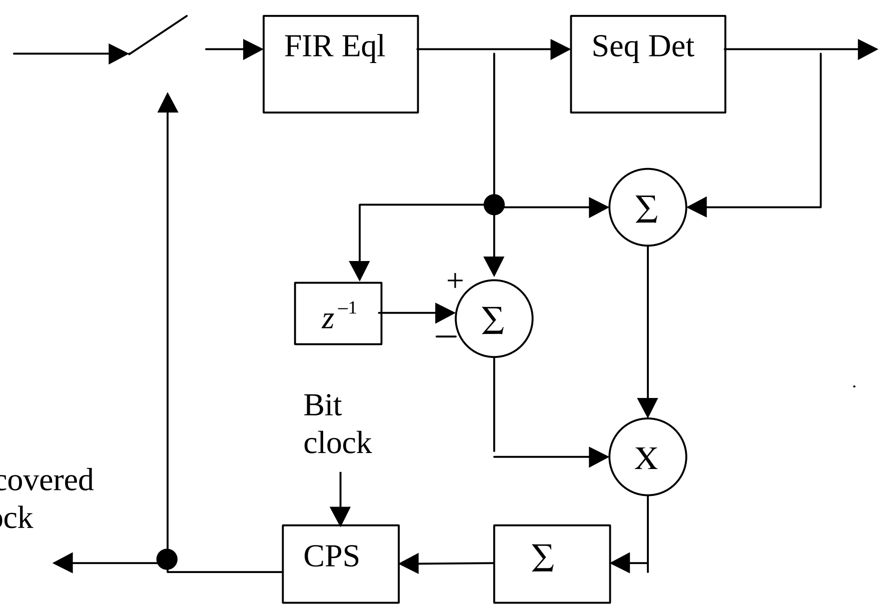

Figure 1. Maximum Likelihood Timing Estimation and Clock Recovery

The difference between two successive samples at the output of the equalizer are multiplied by the error signal, and this phase error is accumulated over N sampling intervals. After N samples, the accumulator sends that value to a clock phase shifting (CPS) network that retards or advances the phase of the bit clock (sampler). The sign and magnitude of the phase shift is directly related to the phase error accumulated over N sampling intervals. The CPS is a tapped delay line made up of delay elements (gates) that have a gradation of ϕ = Ts/M, where Ts is that sampling interval of the bit clock. The number of sampling intervals N that the phase error is accumulated over and the step size of the phase change (1/M) introduced by the CPS will initially be chosen and then refined based on experimental results. An optimal combination of M and N will be chosen to yield the best overall system performance during software simulation.

DC Restore

The signals read from tape may have DC content which biases the values that are compared to the stored sequence values in the detector. A snapshot of the DC content is taken when the stored response in the sequence detector whose Euclidean distance is closest to that of the received sequence are subtracted ($\varepsilon = \Sigma\{d(m) - y(m)\}$). This error ε and its predecessor in time are used to adaptively update a *bias* that is subtracted from the incoming signal to remove DC content. The form of the bias is given below :

$$bias_k = bias_{k-1} + \Delta\varepsilon_k + \delta(bias_{k-1} - bias_{k-2})$$

Here the parameter Δ is a step size parameter that controls how quickly the bias can grow or decay, and δ controls the rate of growth or decay. It is possible that for slowly varying fluctuations in DC offset, δ may be set to zero.

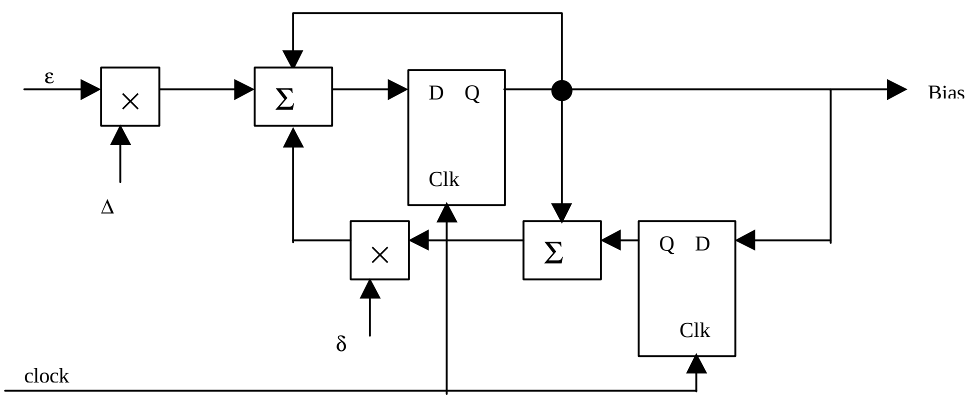

Figure 2. DC Restore

Like timing recovery, the detector output is used in the formation of bias signal, therefore DC Restore is also decision directed. The step size Δ and rate δ will be chosen experimentally to optimize performance.

Gain Control

Any long-term variation of the signal's amplitude will obstruct the sequence detector in its attempt to best fit the curve it has received with target curves that are stored in its memory. A method for monitoring and controlling variations in the signal's amplitude is necessary for optimal decoding of data played back from tape. To control signal expansion and compression, the algorithm graphically described by Figure 2. is used. In this case, the error signal ε is described as

$$e = \sum_m (d_m{}^2 - y_m{}^2)$$

where this energy difference is a subset of sequence detection, and can be exploited to encompass gain control. The bias signal formed from this error is multiplied by the preceeding equalizer taps and added back to form coefficients whose new values account for a change in gain.

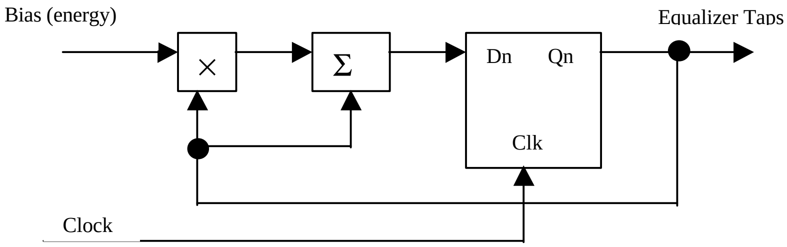

Figure 3. Gain Control by Modifying Target Sequence with Energy Bias

In Figure 3 the energy bias is used to attenuate or amplify the coefficients stored in the equalizer taps and as a consequence adapt to variations in signal gain or attenuation.

SUMMARY

The combination of timing recovery, DC restore and gain control complement adaptive equalization and maximum likelihood sequence detection [1] to optimally decode data read back off magnetic tape. All three operations, timing recovery, DC restore and gain control work to minimize the MSE or energy difference between the received and expected signal, and are hence decision directed. The extent of phase error accumulation N and phase gradation ϕ in timing recovery, and the step size Δ (plus rate δ) used in forming a bias in both DC restoration and gain control are free'parameters whose values are chosen and refined based on experimental results.