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TO: K. Young
 FROM: A. Whitney, J. Goodman
 SUBJECT: SMA Correlator DSP Software

References:

1. Mark4 Memo #239.1 "Definition and Management of Correlator Board DSP routine" Whitney, A.R, Goodman, J.I., 20 October 1997

This memo describes briefly the proposed table structure and theory of operation for collection and accumulation of correlator frame data by the DSP chip on the correlator board.

CNWD	ROUTINE
8	<i>DSP_demux_data</i>
9	<i>DSP_zero_array</i>

DSP_demux_data

The *DSP_demux_data* task is used to recombine correlated time division multiplexed data. The Cell Pointer Table (CPT) holds 512 addresses that point to the starting address of lags contained in each of the 512 cells on the board. The Walsh Pointer Table (WPT) will hold 1024 words (for a 32 phase Walsh Cycle) that point to one of four Walsh phase buffers in which data is accumulated. The Data Collapse Table (DCT) holds 16 words that correspond to the starting offset in a Walsh phase buffer where each cells lags are accumulated. Table 1. Illustrates the format of the *DSP_demux_data* TCB:

				WALSH CYCLE		WALSH INDEX	
	I	MEM_ID	CELL POINTER TABLE (CPT)				
	I	MEM_ID	WALSH POINTER TABLE (WPT)				
	I	MEM_ID	DATA COLLAPSE TABLE (DCT)				
31	24	23	16	15	8	7	0

Table 1: TCB for *DSP_demux_data*

where

Word	Bits	Name	Explanation
4	7-0	WALSH INDEX	Index into Walsh pointer table that denotes the current phase of the Walsh cycle
	15-8	WALSH CYCLE	Length of Walsh cycle
5	23-0	CPT	Pointer to table of pointers to chip cell lags <u>Organization of CPT</u> : Starting from Chip1, Cell 1 and running to Chip 32, Cell 16, each entry points to the start of 33 raw lags read from each cell
6	23-0	WPT	Pointer to table of pointers to accumulation phase buffers <u>Organization of WPT</u> : Starting from Chip1, Walsh Cycle1 and running to Chip 32, Walsh Cycle N , where N is the number of phases in Walsh cycle period
7	23-0	DCT	Pointer to table of template values holding offsets from start of Walsh buffer where data from each correlator chip is accumulated <u>Organization of DCT</u> : Entries 1-16 corresponding to Cells 1-16 that hold value 0,1,2 or 3, corresponding to a subset of 32 lags contained in the particular cell

Table 2: Explanation for *DSP_demux_data* TCB

DSP_zero_array

The *DSP_zero_array* task is used to initialize a phase buffer with zeros at the start of each new Walsh Cycle

ARRAY INC		ARRAY_SIZE					
		I	MEM_ID	ZERO ARRAY (ZA)			
31	24	23		16	15	8	7
							0

Table 3: TCB for *DSP_demux_dat*

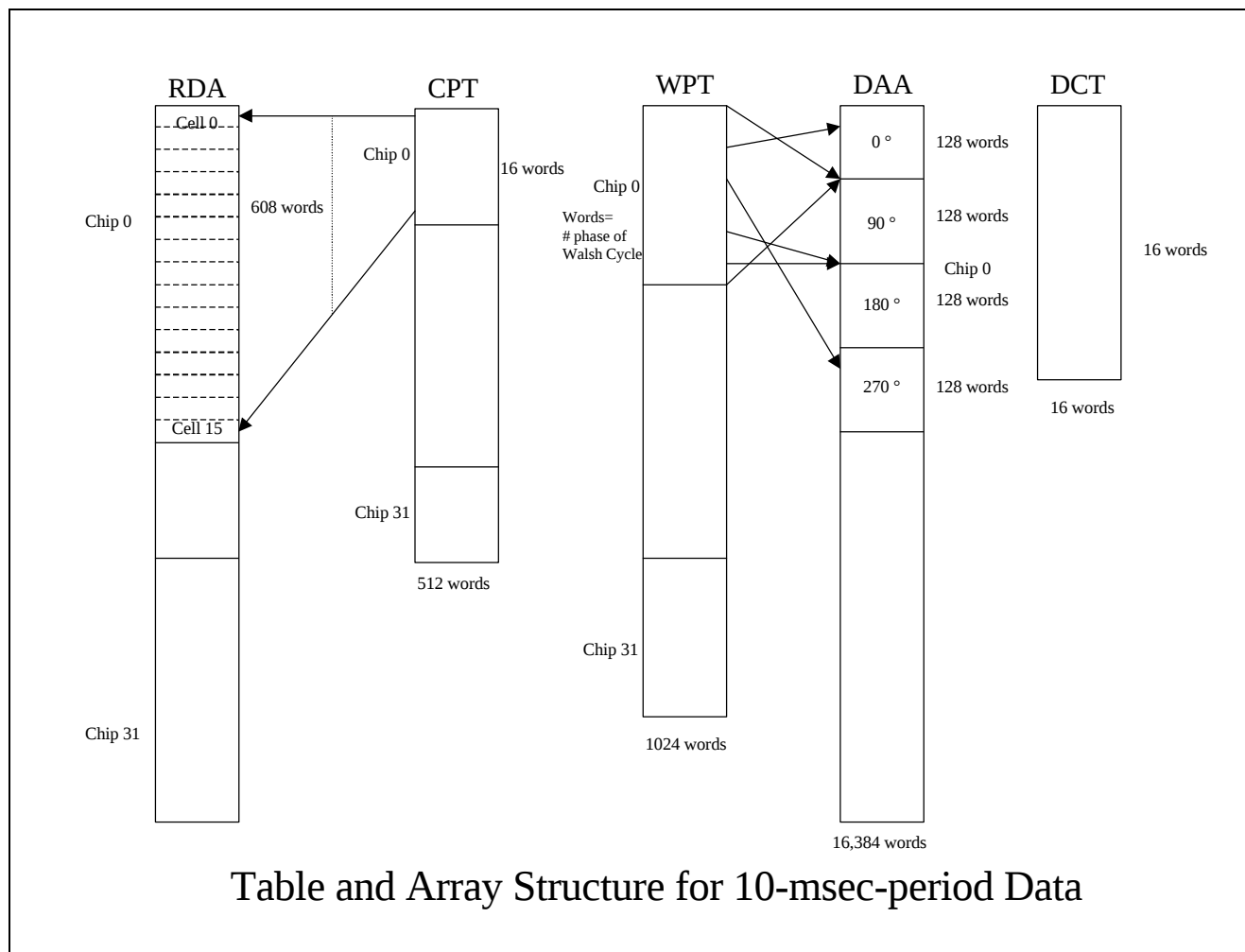


Table and Array Structure for 10-msec-period Data