

**MASSACHUSETTS INSTITUTE OF TECHNOLOGY**  
**HAYSTACK OBSERVATORY**  
*WESTFORD, MASSACHUSETTS 01886*

January 14, 1999

*Telephone: 978-692-4764*  
*Fax: 781-981-0590*

To: Mark IV

From: Hans F. Hinteregger

Subject: Progress report on thin-film head development - **(as of 7 April 1998)**

**1. FEASIBILITY TESTS OF THE THIN-FILM HEAD PERFORMANCE**

**a. Low Error Rate Read Demonstrated**

Using one of the Phase 1 'feasibility' Seagate Peregrine magneto-resistive (MR) thin-film head-arrays, a thin tape [Quantegy 741] pre-recorded at 56 kfc i with a standard inductive VLBI write head has been successfully read with excellent results. Error rates of a few times  $10^{-6}$  were achieved, which is as good as we have ever seen with any inductive head under any circumstances.

**b. Modified Equalizer**

Empirical modification of the standard 80 ips equalizer was required to obtain these error rates: the integrating capacitor was doubled, and the midband coupling resistance tripled. Further optimization of the equalizer is possible but has not yet been attempted.

**c. MR Preamp and Test Interface**

The dual-bar head assembly was interfaced with a Silicon Systems 32R1574R MR preamp designed for 22-85 ohm heads. The MR heads are about 60 ohms. One of the complementary outputs of this x150 gain amplifier, resistively divided by 2 for a net gain of x38, was coupled to the input of the 3467 video amp that drives the equalizer in a Mk3A read board. The zero-crossing detector output of this board replaced the 'A' monitor channel of the Haystack Mk3A data-acquisition drive on its way to a Mk3 decoder.

**d. High Tape-Noise-Limited SNR**

The SNR with the 12um-wide MR head is heavily tape-noise (TN) limited, unlike the SNR of the 38um-wide inductive read head which is electronic-noise (EN) limited. When the SNR is TN-limited, SNR is reduced 3 dB for each halving of the read-head width; when the SNR is EN-limited, the SNR is reduced by 6 dB for each halving of the read-head width. For 56 kfc i at 80 ips, the 2.2 MHz 'bandedge' SNR of the MR heads was measured to be typically 26-28 dB, while the SNR of inductive read heads is typically 18-21 dB. This indicates that even though the MR read head is less than 1/3 the width of the inductive read head, the SNR improvement is somewhat more than 6 dB; in other words, the MR read-track width could be reduced by another factor of 4 before the SNR would drop to that of the current inductive read head.

#### e. Double Linear Density Potential

A double-density recording [114 Kfci, on the same Quantegy 741 tape] was also examined at 40 ips using the same modified equalizer. Though the zero-crossing detector cannot decode the partial response signal, an average SNR over the band of 21 dB was noted. This is thought to represent at least 6 dB margin for good double-density performance. The equalizer approximately flattened the tape-noise spectrum, and the three-level eye pattern of the signal appeared to approximate the PR4 [partial response class 4] target response - for which detector ICs are available.

#### f. Write Performance

The Peregrine TF write head has a gap length of 1.0  $\mu\text{m}$  and is 38  $\mu\text{m}$  wide (compared with the 12  $\mu\text{m}$  wide TF read head). The relative write loss of the TF write head at the 56 kfci bandedge was found to be 6 dB compared with the standard ferrite head with 1/3 the gap length. This 6 dB loss is roughly equivalent to the gain achieved by reading with the MR heads, and suggests that, if the TF write-gap length can be reduced to  $\sim 0.3 \mu\text{m}$ , that  $> \sim 100$  kfci bit densities can be successfully supported with the TF head array. Reducing the write gap length should require only changing the gap spacer material deposition time and no new masks. As noted below, we are therefore hoping that Seagate will agree to supply, near the end of prototype phase 2, at least some bars with a shorter ( $\sim 0.3 \mu\text{m}$ ) gap length. This will allow us to complete a VLBI high linear-density 'write-feasibility' check. We will also try get assurance that a short-gap version of otherwise standard wafers will be available for VLBI implementation, even if only once for a 'lifetime' supply.

#### g. Head-to-tape Contact

The output of the MR head was found not to depend significantly on tape speeds from 20-320 ips. This indicates good contact at both edges of the flat contour. There is, however, an indication of a constant 'excess' spacing loss at the active read and write elements; this will not affect SNR at 80 and 160 ips, but does have some negative impact at 320 ips as the ratio of tape-to-electronic noise diminishes. It is anticipated that this 'excess' spacing will be significantly reduced in the future by using a wider flat surface on the head array, which is planned for Phase 2.

## 2. DIGITAL READ-CHANNEL DEVELOPMENT

The current Mark3 tape recorders are able to read data from tape at a maximum density of 56 kfci. Pseudo-random data recorded on a Mark3 data-acquisition system at 84 kfci ( $84 \text{ kfci} = 1.5 \times 56 \text{ kfci}$ ) was played back through standard equalizers and digitally sampled at high speed. Digital data corresponding to approximately 45,000 recorded bits were captured on floppy disk and played back through a software model to remove the effect of the current analog equalization. The unequalized data, representing only the response of the inductive head and pre-amp, were processed in software using maximum likelihood sequence detection (MLSD) in conjunction with optimal timing recovery and gain control. There were no detected errors. Extensions of this technique are applicable to densities as high as 112 kfci by augmenting the current algorithm to handle data-dependent noise.

The model used to decode the data is very simple, a 4 state MLSD, digital timing recovery with 4 multipliers and adders, and gain control with 2 multipliers and adders. Equalization (adaptive or fixed) will only enhance performance, and in all likelihood is not necessary at this density. Implementing a single channel in hardware in a standard FPGA should not pose severe technical difficulty or risk.

Further details on these initial encouraging results are provided in Mark IV Memo #256, 15 January 1998.

### 3. SEAGATE PARTNERSHIP

Seagate maintains its commitment to deliver prototype Phase 2 thin-film head-arrays for our project. However, commercial production plans for the Peregrine format head-arrays have been recently replaced with a new Seagate/IBM/Hewlett-Packard joint-venture format. The new array has fewer channels than the 16 read-write channels of the quarter-inch Peregrine array, but it can still be made compatible with the VLBI requirements in row-bar form. It is expected that this format will go into volume production, and thus satisfy VLBI's desire to use a commercial product. The first round of joint-venture format wafers already exist and, as described below, we are negotiating with Seagate on their use for the early mechanical design and integration part of phase 2.

It is now expected that the new thin-film head bars can be supplied for the prototype phase, processed and packaged in a manner similar to that employed for the Peregrine format. A new flex interconnect has been designed. Whether it can be used in a VLBI implementation package still needs to be determined. The plans that we are discussing with Seagate for the Phase 2 prototype delivery are as follows:

#### 1. Delivery of 1-inch Long Bars To Obtain A 64-Channel Head-Array:

Seagate has offered to provide Haystack monolithic, 1-inch long, flat-lapped bars, with the new joint venture format. This is a desirable situation from our stand point as it eliminates the work required to transform the new joint-venture head format to a form useful for 1-inch wide tape operation.

The new bars will contain several islands of head groups placed a certain pitch distance apart. Each individual head in these head-groups will have similar sizes to the Peregrine heads. However, the pitch between these groups of heads is such that we need to use three bars (with a total of 74 channels) to obtain 64 simultaneously-working channels, and thus meet the Mark 4 1-Gbps data-rate requirement. The 74 channels will be distributed almost uniformly across the inch-wide tape. Some channels will be redundant, in addition to the redundancy of 10 'extra' channels. In the previous phase of the project, we gained valuable experience in constructing head arrays with a dual assembly of 1-inch bars. Assembling three bars in an arrangement to replace the current VLBI head-stack is within our capabilities.

#### 2. Reduction of the write-gap length:

The write gap length of the new heads will be the same as that tested in the feasibility Phase. But as described in section 1f above, our tests have shown that this 1 um long write element barely meets the VLBI requirements. We know that a write element length of 0.3 um, as in the current VLBI heads, would meet the requirement, but we have been informed by Seagate that the migration path of the new standard heads does not consider a shorter write element in the near future. We are therefore presently inquiring whether Seagate would be willing to supply some bars with a shorter gap length (~0.3 um), as the second half of the prototype phase deliverables on a special wafer run. There is no agreement at present for such a deliverable.3. Summary of requested deliverables: Based on the above, we are requesting from Seagate the following deliverables for the prototype phase:

- a) Six 1-inch long bars with the standard 1 um-long write elements. Delivery in early summer 1998. This will allow us to assemble three bars to test the 64 channel head arrays. The other bars can be used for a second array unless they are used as spares in the construction.
- b) Six 1-inch long bars with 0.3 micron long write elements. Delivery could be delayed till late 1998, pending agreement on the special wafer run that this requires.

These heads will also have the proper flex-circuit attachments, and a flat-contour. The task of assembling the head arrays will be shared between Haystack and Seagate. The lapping of the heads and attaching the flex-circuits will be performed by Seagate. Evaluation of the performance of a 64-channel head at Haystack requires new electronics. Design and production of prototype parallel read/write, write driver and MR preamp boards will start as soon as possible.