MARK IV Memo #278

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
HAYSTACK OBSERVATORY

WESTFORD, MASSACHUSETTS 01886
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Telephone: 978-692-4764
Fax: 781-981-0590

TO: Mark 4 Development Group
FROM: Alan R. Whitney and Roger J. Cappallo
SUBJECT: Specification for Mark IV Decoder Module

Introduction

The venerable Mark III decoder has now seen service for almost 20 years(!) and is badly in need of an upgrade. The Mark 4 Decoder Module is intended to be a *plug-compatible replacement* for the Mark III decoder, but with the following *additional* features:

1. Support the full 18 Mb/s data rate of the Mark 4 track-recording-rate.
2. Significantly expand the size of the data buffer; expand data-buffer interface to include a SCSI port as well as a high-speed serial connection.
3. Process 4 channels of raw-sampled data from the Mark IV formatter to extract phase-calibration phases and amplitudes in a flexible manner.

A Mark 4 correlator chip will be responsible for phase-cal tone extraction from up to 4 selected channels of raw sampled data available from the back panel of the Mark IV formatter, or one of the two decoded-track channels. The capabilities of the correlator chip allow considerable flexibility as to the manner of data processing to extract the tones, as well as the simultaneous extraction of the amplitude and phase of many tones. The phase-cal processing algorithm can be chosen to be either the simple algorithm used in the Mark III correlator, or a more complex algorithm proposed by Sergei Pogrebenko (EVN memos 2 and 8) which allows simultaneous extraction of all tones in a BBC channel using the capabilities of the correlator chip.

A single-chip micro-processor will act as the command and control center, as well as perform some modest amount of processing in support of the decoding and phase-cal-extraction functions.

Functional Description

The function of the Mark IV decoder is perhaps most easily understood by reference to the suggested front panel in Figure 1 plus the block diagram of Figure 2.

Display

The display is a backlit LCD with 4 lines of 20 characters each.

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Display Modes

The desired display mode is selected by repeatedly pressing the 'Mode' button, which cycles through the display modes. The available display modes are as follows:

1. 'A' - displays information derived from tape-track channel A.
2. 'B' - displays information derived from tape-track channel B.
3. 'FRMTR' - displays information derived from four channels of raw-sampled data from the Mark IV formatter.

In the 'A' and 'B' modes, the following information is continuously displayed for the selected channel (see Figure 1):

- 'Time' - decoded time/CRC information. The 'Freeze' button allows the user to 'freeze' the display at a random time to examine, for example, the validity of lower-order time digits. The display is 'frozen' whenever the 'Freeze' button is pushed and held; normal display resumes upon its release.
- 'Aux Data' - displays the current decoded auxiliary-data field. The display is frozen whenever the 'Freeze' button is depressed and held; normal display resumes upon its release. When the 'Freeze' button is depressed, the 'Time' and 'Aux' data displayed are from the same tape frame header.
- 'Errors' - displays four 4-digit error counts for each decoded channel, labeled as indicated in Figure 1; counts are cleared when 'Clear' button is pushed; error counting resumes when released. For consistency with the old Mark III decoder, the displayed parity-error count will be the number of parity errors over sequential intervals of 400 (default) tape frames; all other error types will simply accumulate; however, the parity-error count available to the MAT will simply accumulate until read. If error counts exceed the available display field, the error count divided by 1000 (and properly rounded) will be displayed, followed by a 'k' (e.g. 35kP indicates ~35000 parity errors).
- 'PCAL' - extracts 10 kHz phase-cal amplitude and phase from the decoded data stream and displays results. Results will be updated once per (local wall-clock) second. In order to properly extract the 10 kHz phase-cal tone for arbitrary data, the record-time track data rate must be known. This can be determined (and displayed) by examining the decoded frame times from two successive frames.

In the default 'FRMTR' mode, each line of the display will show the phase and amplitude of one of the four sample-data streams from the Mark IV formatter.

Special software may also be present within the decoder to extract other information, such as

1. Phase-cal frequencies other than 10 kHz.
2. State counting of 2-bit data
3. Power spectrum of 1 channel

4. Other special processing modes using the Mark IV correlator chip.

In the case of special processing, the display format is unspecified. However, it is suggested that some indication be given that the display is not operating in a default mode, such as by intermittently flashing a front-panel LED or other indication.

Note: At any given time, the correlator chip will be restricted to operating only on data in the selected display mode.

Errors

Four types of errors are displayed for each of the decoder channels A and B. Upon the occurrence of each type of error, the corresponding LED will illuminate for *one full tape frame*. The detected error types are as follows:

- 'Parity' - parity error threshold (software settable, default=0) exceeded in preceding tape frame.
- 'NoSync' - detection of a missing 'sync' word (i.e. sync word not detected where expected) in the preceding tape frame.
- 'ReSync' - detection of unexpected sync word in the preceding tape frame.
- 'CRC' - detection of cyclic redundancy code error (in Mark III tape frame header) in preceding tape frame.

Monitor Outputs

Three BNC monitor output jacks are available from each of the decoder sections A and B. All levels are TTL. The outputs are as follows:

'Clock' - clock corresponding to 'Data' (blanked during parity bit); this clock signal is also active during the tape-frame header.

'Data' - recovered data from corresponding decoder; complete Mark III frame is presented, including header and parity bits.

'Frame Sync' - pulse corresponding to Mark III frame header, used mostly for scope synchronization when observing 'Data'

Data Buffer

Upon command from the MAT, either of the following data may be captured to RAM buffer memory:

1. The A-decoded data stream: Data-capture will be initiated on the first decoded 10-sec tick following the MAT command to arm the buffer. All tape-data frames, including all the entire header and parity bits, will be captured. Data collection will continue until the RAM memory is filled (~64MB) or a MAT command is issued to terminate capture.
2. A single selected channel of 2-bit/sample data from the formatter. A pre-capture decimation ratio of 2^n ($0<=n<=255$) may be chosen. Data-capture will be initiated on the first formatter-1-pps tick following the MAT command to arm the buffer. Data collection will continue until the RAM memory is filled (~64MB) or a MAT command is issued to terminate capture.

Readout of the captured data may be either through a high-speed serial port (at 115 kbaud) or a single-ended SCSI-1 port on the rear of the module.

Due to the potentially high-bandwidth requirements of the data-capture process, other decoder processes may be suspended during the buffer-capture process.

Specification

Back panel

Rack connector:

Power: +5V, -5.2V

Communications: MAT (RS-423) bus, with address set by jumpers on back-panel connector; 7 data bits, even parity, 2 stop bits

Data: 2 tracks of read-after-write data from tape recorder, each with accompanying clock; maximum bit rate is 18 Mbits/sec per track (ECL)

Cable connector:

4-channels of raw-sampled 2-bit data, always at 32 Msamples/sec (ECL)

32 MHz clock (ECL)

1-pps timing tick (ECL)

9-pin D female:

RS-232 interface for program development/debug/download.
Same pinouts as connector on standard modem.

9-pin D female:

RS-423 interface for data-buffer readout; 115 kbaud max.
Same pinouts as connector on standard modem.

SCSI-1 single-ended 50-pin connector and daisy-chain connector.

For reading data-buffer data

Phase-Cal Processing

Phase-cal tones may be extracted by processing through the Mark IV correlator chip. As indicated in Figure 2, the data source may be either the Mark IV formatter or the on-board decoder. The primary differences are as follows:

Data from formatter - The data from the 4 selected channels always arrives at 32 Msamples/sec with 2 bits/sample, and is accompanied by a 1PPS tick. The correlator chip may extract phase-cal from all 4 channels simultaneously.

Data from decoder - The decoded data from channel A/B is 1-bit only (presumably sign), and can be selected to replace USBx at the input to the 4x4 mux, as indicated by Figure 2; in this mode, the ‘magnitude’ bit into the 4x4 mux must be held constant (at ‘0’ or ‘1’, depending on coding). Maximum data rate of decoded bit stream is 16 Mbits/sec. A ‘1PPS’ pulse is issued from the decoder on each *decoded* second tick; 1PPS may be absent under error conditions. In addition, the ‘CLK’ signal from the decoder is quiescent during each parity-bit period.

Control signals to the correlator chip

The simplified timing diagram and block diagram of Figures 3 and 4 show the control signals necessary to drive the correlator chip:

BOCF:

Period: Selectable to specified $n \times$ 125,000 sample intervals, where $1 \le n \le 256$.

Length: 256 clock cycles

Note: Period of BOCF will always be chosen such that there are an integral number of correlator frames within a 1PPS period.

ENADD:

Period: 2^n clock cycles, $0 \le n \le 7$; n=0 corresponds to continuous ENADD=1

Length: 1 clock cycle

Phasing: Phased so that first sample after falling edge of BOCF always has ENADD=1.

ENSHFT:

Period: 2^n clock cycles, 0<=n<=7; n=0 corresponds to continuous ENSHFT=1

Length: 1 clock cycle

Phasing: Phased so that first sample after falling edge of BOCF always has ENSHFT=1.

Responsibility of microprocessor:

Setup correlator chip and timing and control according to processing mode commanded by user.

Read data and status from correlator chip every BOCF cycle and process according to specified algorithms (TBD).

Send results to user as appropriate.

Notes

State Counter

A state counter can be built by selecting the same data stream to all four mux outputs, and then controlling the validity bit stream according to state as indicated in Figure 2. Four correlator cells of the Mark IV correlator chip can then be used to count the four states by reading the 'global validity counter' in each of the cells.

Decoders

Note that the A and B decoder channels are completely independent; this is required since the playback from two tape tracks is generally skewed by some number of bits (up to several hundred). Consequently, though both decoders operate simultaneously, only the data from one or the other may be directed to the correlator chip or to the data buffer at any given time.

Response to Sync Errors

When extracting phase-cal from a decoded tape-track channel, various sorts of errors may occur. The control of the correlator chip must be designed so as not to produce an unacceptable 'hiccup' (in particular, a short correlator frame) in the normal data flow through the correlator chip. Figure 4 shows a simple block diagram of a BOCF control circuit which will prevent such hiccups and that will also automatically resynchronize to a 1PPS tick. In the absence of 1PPS, the control circuit will simply flywheel.

Restrictions on Simultaneous Functions

In order to simplify software and keep the processor load to a reasonable level, the data-buffer function (both capture and readout) and any use of the correlator chip are mutually exclusive. Furthermore, some high-bandwidth data-capture modes may require suspending other decoder functions during data-capture activity.

Communications Protocols

For all functions with counterparts in the Mark III decoder, the MAT communications protocol should be identical, if possible; the will allow the Mark IV decoder to replace the Mark III decoder as a fully backwards-compatible unit. For new functions of the Mark IV decoder, the communication protocol is as yet unspecified.

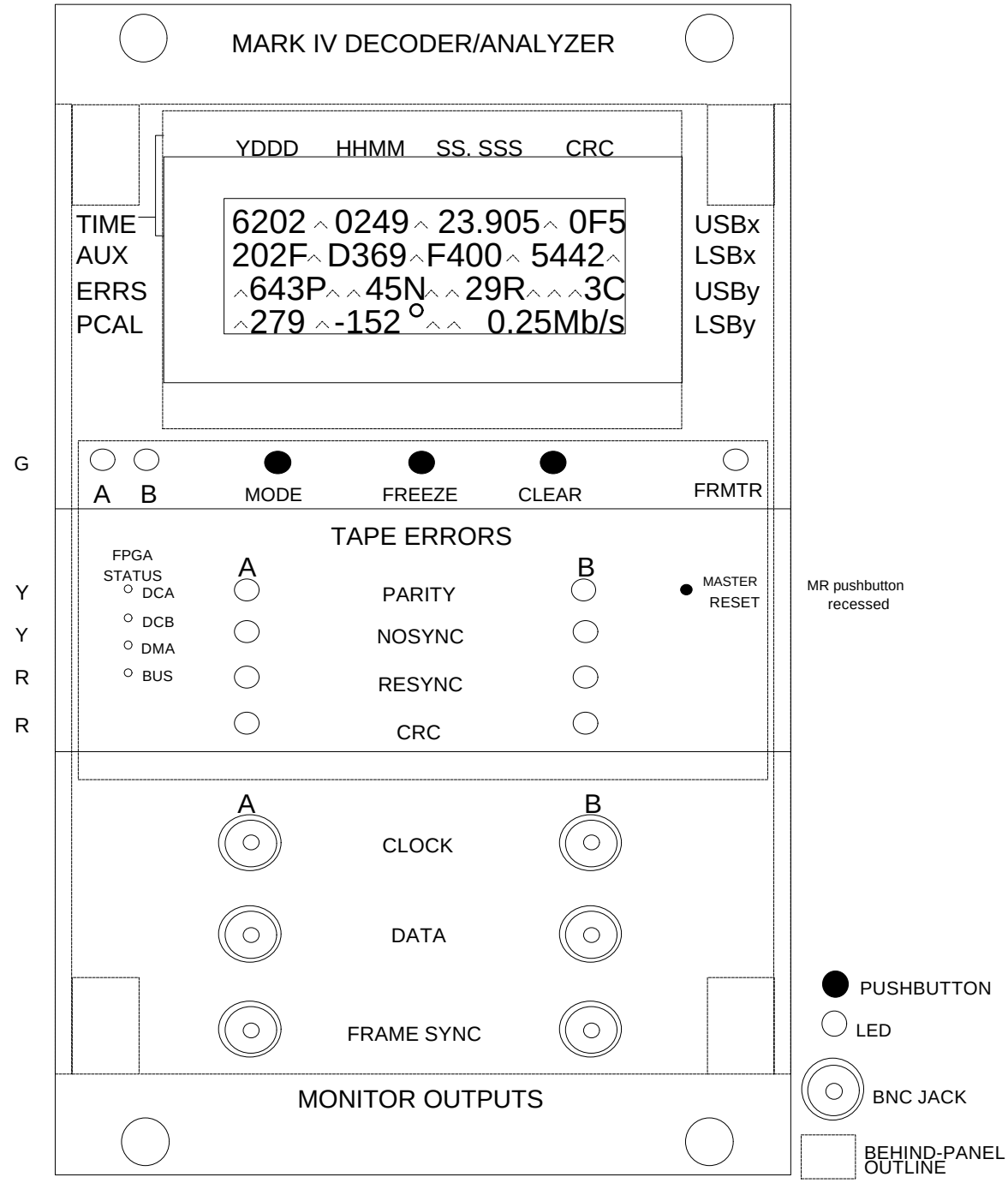


Figure 1: Mark IV Decoder Module Front Panel Layout

ARW 3 APR 00
FPANEL.DRW

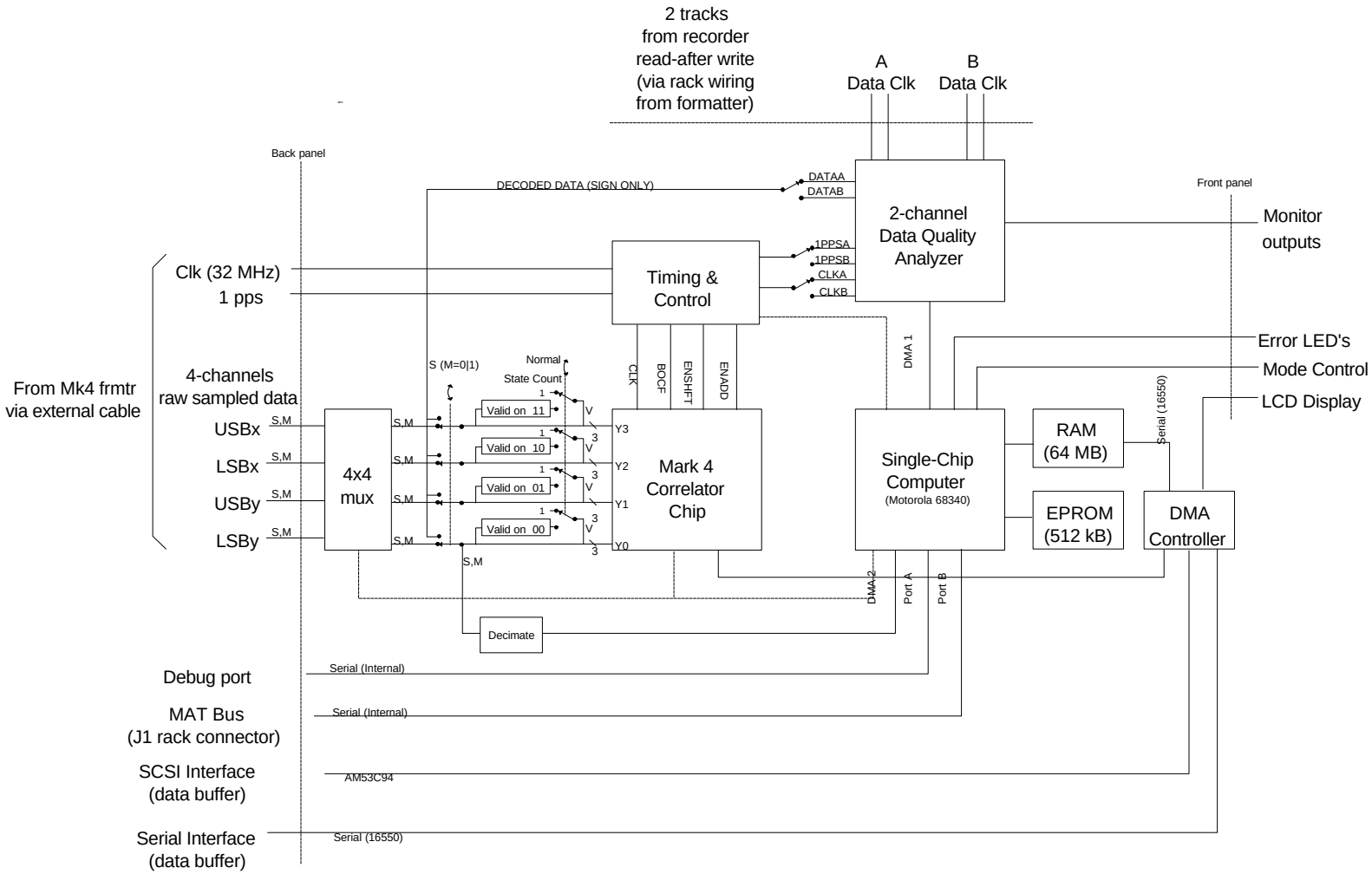
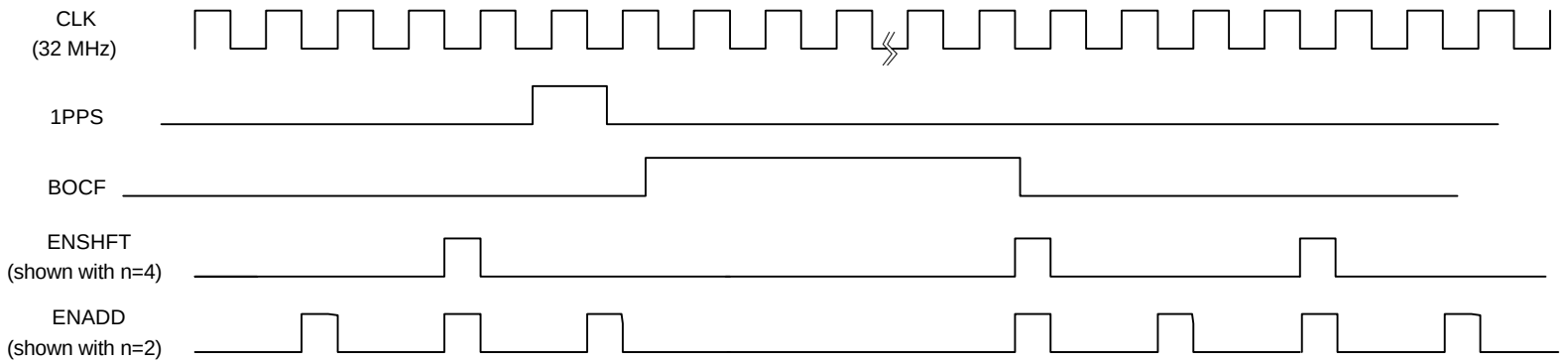


Figure 2: Block Diagram of Mark 4 Decoder Module

ARW 24 Mar 00
DECODER.DRW

Using data from formatter:



Using data from decoder:

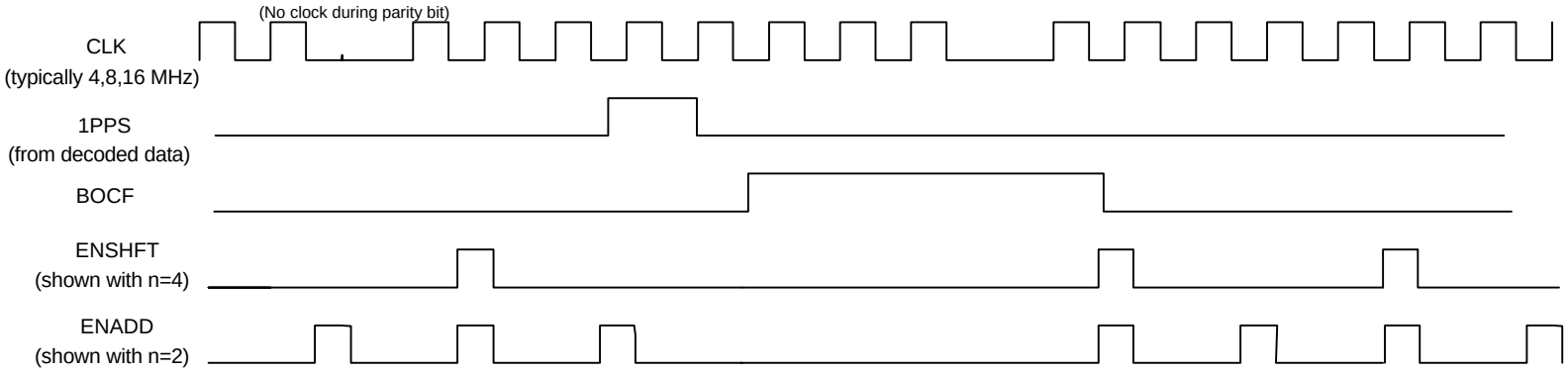


Figure 3: Simplified Timing Diagram

ARW 24 FEB 97
TIMING1.DRW

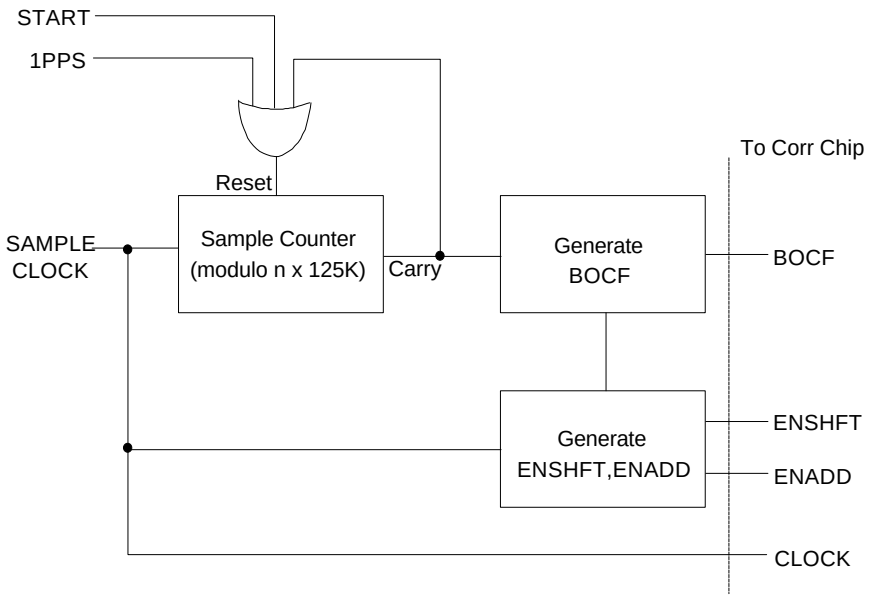


Figure 4
Correlator Control-Signal Generation Block Diagram (simplified)

ARW 000403
TIGO2.DRW