MASSACHUSETTS INSTITUTE OF TECHNOLOGY
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS 01886

Phone: (978) 692-4764
Fax: (781) 981-0590

16 March 2001

To: List

From: W. Aldrich

Subject: Mark IV Correlator Board Timing

A Marginal timing condition has been found to exist on the Mark IV correlator board. The condition affects the timing of the control signals ENSHFT, ACCUM, and BOCF as they enter the correlator chip. With current timing control jumper settings, a hold time violation was found to exist as is illustrated in the timing diagram below for the case of ENSHFT.
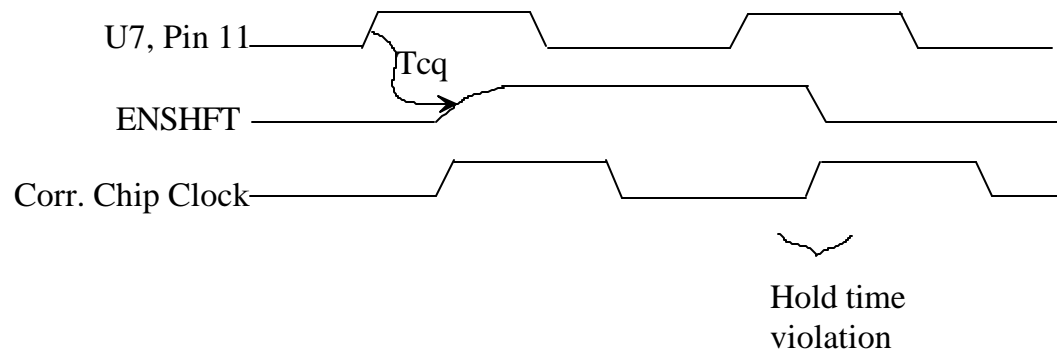
Experience on the Mark IV correlator at Haystack has found that this situation is most apparent in its affect on headers. It causes an occasional loss of the ENSHFT signal when data is being decimated. Because headers are more highly encoded than the data stream, a failure to shift a header bit into the chip will usually cause the header to be detected bad. The effect on correlation data is more subtle and is more difficult to detect. (It effectively causes a data sample to be lost from each stream entering the chip.)

Fortunately, there is a minimally invasive cure for this problem which involves changing the skew control jumpers on a clock buffer. The change will delay the buffer clock with respect to the correlator chip clock and effectively trade setup time (of which there is plenty) for hold time.
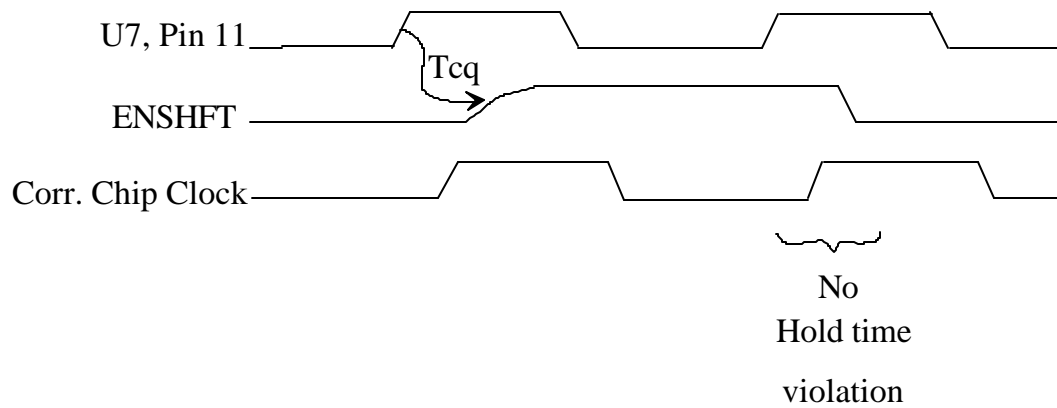
Currently, jumper J30 is set to "high" and jumper J29 is set to "low". This causes the clocks CLKA1, CLKA2, CLKA3, and CLKA4 to be skewed 4 TU early (about 4.8 ns.). We have changed the setting so that J30 is set to "low" and J29 is set to "mid". (Remove the jumper.) This reduces the early skew of the clocks to 2 TU (about 2.4ns.).

All of the correlator boards in the Haystack Mark IV correlator have been adjusted this way. No "header loss" symptoms have been observed in running the correlator for about one week. Although it is possible to observe the timing of the signals in question with a suitable oscilloscope (bandwidth about 500 MHz.), the replay of a decimating correlator run which has suffered header loss before the jumper change may be an easier validation of the change.

Before

U7, Pin 11

Tcq

ENSHFT

Corr. Chip Clock

Hold time
violation

After

U7, Pin 11

Tcq

ENSHFT

Corr. Chip Clock

No
Hold time

violation

List:

W. Alef
A. Bos
J. Buiter
M. Dexter
A. Freihold
K. Kingham
S. Parsley
M. Wunderlich
A. Whitney