MARK 5 MEMO #030

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Subject: Delay Calculations for the Mk5B DOM

Background

The Mk5B DOM has several functional elements that affect the delay of the data stream it produces. There is a large (notionally circular) RAM buffer that holds 64 M data samples. It is supplied with data from the StreamStor (SS) card, and read out via a read pointer whose value is set under software control each correlator frame (CF). The initial data from the SS card is selected by high level software control of a byte pointer, but once the flow is established, the data words are sequential. After the data stream exits the RAM buffer it passes through logic that can duplicate or delete samples, under control of the delay generation hardware. This delay generator has three parameters, which are also set by software control for use at the beginning of each CF. The parameters are a fractional bit delay error, the associated error rate, and a rate sign bit controlling whether samples are skipped or duplicated.

The host software is supplied via messages with high level parameters that are used to set the hardware registers to appropriate values. These parameters include the starting byte number at which the SS disk subsystem should be read for loading the circular buffer, and quintic spline polynomials for calculating the linear delay parameters. In another use unrelated to the delay calculations, the splines are also used to form the header packets that are spliced into the data stream. A set of subroutines, called via *header_gen ()*, are used to generate the delay model and the header packets, given the splines as inputs.

Calculations

For each CF, *header_gen ()* should be called with the appropriate ROT. Due to pipelining within the correlator chip, there is an offset of 2 CF's between calculation of header data and its use. Thus, if header data are being calculated immediately after a CF interrupt at time t, the time argument supplied to *header_gen* should be set to $t + 2 * cf\_len + \Delta t$, where *cf_len* is the length of the correlator frame in sysclk's, and Δt is the length of the

(possibly stretched) correlator frame header. This latter term is necessary since the delay and phase model generators only begin incrementing at the end of the correlator frame header.

The returned values of d_fract[] have been defined so that the resulting binary fields can be written directly to the Mk5B delay generator registers. Specifically, d_fract[0] is the fractional delay error in samples, multiplied by 2^{32}. Its value has been modified for direct use in the hardware: it is expressed as a positive delay, and biased by 0.5 sample in order to make the shift happen at an error of +/- 0.5 sample. The value in d_fract[1] is the delay error increment in units of samples per sysclk, also converted to be a positive quantity. The sense of the delay shift – whether it is a skipped or duplicated bit – is controlled by the most significant bit. The values can be used directly to preload the DOM delay generator at locations 4000 – 4003.

For the record, the calculations within header_gen () are given here. If we define e to be the fractional bit delay error, in the interval [-0.5, 0.5], and δe to be the rate of change of e, expressed as an increment per sysclk, then d_fract is calculated as follows:

$$d\_fract_0 = 2^{32}\left(1.0 - \left|0.5 sign(\delta e) - e\right|\right)$$

$$d\_fract_1 = \left|\delta e\right|$$

with bit 31 of d_fract_1 set iff $sign(\delta e) > 0$.

The delay generator will track the delay during a CF, duplicating or skipping samples as needed, but at the start of each CF the initial delay must be chosen by loading the value of the circular buffer read pointer (i.e. *sdram address*, in locations 0005 – 0006). The ability to change the delay at the start of each CF allows the system to have greater flexibility, for example by transitioning from one scan to the next without stopping, by just changing the delay model.

The calculation of the read pointer address must take into account the 64 MS size of the circular buffer, the sample rate, the whole sample delay that is returned from *header_gen()*, and the time. Note that the delay and the time are appropriate for the start of the very next CF, as there is no local pipelining in the DOM. Thus for delay generation purposes, the results from a header packet calculation must be kept around for one CF before it is used within the DOM. The expression for the initial read address is

$$A = \left(\left(t - t_0\right)\frac{f_s}{S} + \tau \right) \bmod 64e6$$

where:

- A is the RAM buffer address
- t is the epoch for the calculation, in ROT sysclks
- t_0 is the epoch of the first sample in this scan, also in ROT sysclks
- f_s is the sample rate in samples/sec
- S is sysclks/sec (= 32e6)

τ is the (whole sample) delay in samples

Note that a second of data "padding" will be read in prior to the start of the scan, in order to insure that the quantity in parentheses will be positive, despite the fact that τ is in general a small ($\leq$ 22 ms) negative quantity.