MARK 5 MEMO #054

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
HAYSTACK OBSERVATORY
WESTFORD, MASSACHUSETTS 01886

Telephone: 978-692-4764
Fax: 781-981-0590

25 April 2007

To: Mark 5 Development Group

From: Brian Fanous

Subject: Dom Station Unit Operation

Initialization

Task	Parameters	Comments
1. 1. Assert PLX reset to DOM.		
2. Turn interrupt propagation from PLX to CPU off.		Clear Interrupt control reg in I/O space. This won't be done once the interrupt handler is working.
3. Dessert PLX reset to DOM.		DOM is initialized to known state. All DOM blocks are disabled. No data flow.
4. Setup RCLK		Set the internal clock to 32 MHz (not necessary for SU with a correlator but won't hurt) using <ICLK Control>. Set the appropriate configuration in the <RCLK PPS Rate Register> : rclk_rate_code = 000; PPS_div_code = 010 for 32 MHz playback; If test mode (no correlator): use_internal_pps = 1 If non-test (using correlator) use_internal_pps = 0 After all that, clear the RCLK_TRISTATE_EN bit in the <DOM CONTROL REG>. Set the the mode field to SU in the same register.
5. Suppress PPSes		Set suppress_pps bit in the <System PPS Suppress Register>
6. Setup BOCF		Write appropriate values to <Correlator Frame Length Reg0> and <Correlator Frame Length Reg1>

7. Enable timing and BOCF generation blocks.		Set the timing_en and bocf_gen_en bits in the <Enables Register>. **RCLK begins at output.**
8. Enable ROT1PPS interrupt		
9. Wait for ROT1PPS interrupt		
10. Unsuppress a pps		Clear the suppress_pps bit in the <System PPS Suppress Register>
11. Wait for a ROT1PPS interrupt		**BOCF begins at output at this ROT1PPS.**
12. Suppress the PPSes		
13. Clear the interrupt mask register		Don't need to see ROT1PPS interrupts for now.
14. Initialize the serial links		Pulse DAV# to VCC by setting QSPARE[1] bit in the <DOM Control Register>, waiting several hundred ms, and clearing the bit.. This step can also be run independently again, after the initialization if there is a need to resynchronize.

Configuration

General Setup:

1. Make sure only timing and BOCF generation blocks are enabled.		Set the timing_en and bocf_gen_en bits ONLY in the <Enables Reg>.
2. Assert reset to all non-running, SU relevant blocks.		In the <DOM Resets0> register set: fpdp_xface_rst, fpdp_fifo_rst, strip_header_rst, sh_fifo_rst, unpack_xbar_rst, xbar_ram_rst, cfdr_rst, cfhr_rst, delay_gen_rst, suo_rst bits. In the <DOM Resets1> register set: sdram_xface_rst, fpdp_dcm_rst bits.
3. Tell StreamStor to start playing appropriate scan.		“play=off”, “set_scan=?” , “play=on”. This starts the FPDP clk but no data flows to the DOM because fpdp_xface_en is cleared.
4. Take the FPDP DCM out of reset now that the FPDP clk is going.		Clear fpdp_dcm_rst in <DOM Resets1>. Now the FPDP DCM can lock to the FPDP clock.
5. Wait 100 ms for DCM lock.		
6. Take all blocks out of reset.		Clear <DOM Reset0> and <DOM Reset1>.

Front End:

1. Configure DOM Front End.	<StreamStor Invalid Reg 0> <StreamStor Invalid Reg 1> <DIM Invalid Reg0> <DIM Invalid Reg1> <Disk Frames per Second> <Xbar Slice Setting RegN> (N=0:31) <Unpack Code Register>	This configures all blocks of the DOM before the RAM buffer. The blocks are not yet enabled. If Phase Cal is implemented, then phase increments are written here.
2. Configure Phase Cal/State Count		*If implemented, phase cal and state count are setup here.*

Back End:

1. Set the Station Unit output data rate.	<SU Output Configuration Register>: suo_prescl bits	Be careful to use a valid value here. This value determines how many RCLKs per output sample.

Initial values for output:

1. Load SDRAM start address	<SDRAM Address0> <SDRAM Address1>	This is the address in the SDRAM that the output data will start from at the end of the next BOCF.
2. Load Delay parameters	<Delay Error Reg0> <Delay Error Reg1> <Delay Rate Reg0> <Delay Rate Reg1>	
3. Load Correlator Frame Header	<Correlator Frame Header RAM Bank A> for CF 0.	First correlator frame header.

Begin filling DOM buffers

1. Wait for SDRAM DCMs to finish locking.		Check Status Register bits DCM0 and DCM1 and sdram_clk_stopped. Make sure the DCM0 and DCM1 bits are '1' and sdram_clk_stopped is '0'. This ensures that the SDRAM clocks work okay.
2. Turn SU output off.		Clear <SU Output Configuration Register> bit suo_run. This will keep data from flowing out of the DOM once blocks are enabled.
3. Turn phase cal interrupts on.		*If phase cal and state count are implemented, phase cal interrupts are turned on here. Phase Cal interrupts will be generated as soon as data begins to flow into the DOM and should be serviced throughout the scan.*
4. Enable relevant blocks in DOM		Enable fdpd_xface_en, strip_header_en, unpack_xbar_en, xbar_ram_en, sdram_arbiter_en, sdram_core_en, sdram_rcvr_en, cfhr_en, delay_gen_en, suo_en, timing_en (should already be set), bocf_gen (should already be set) **This will start data flowing into the DOM.**
5. Wait for SDRAM init/fill to finish.		Monitor sdram_init_done bit in <Status Register>

Begin Station Unit Output

1. Enable the Correlator Frame interrupt		Set the CF_IM bit in the <DOM Interrupt Mask Register>
2. Wait for a CF interrupt		
3. Turn SU output on		Set the suo_run bit in the <SU Output Configuration Register>. **Output will begin on next BOCF.**

While Running

On CF interrupts

1. Load SDRAM start address	<SDRAM Address0> <SDRAM Address1>	This is the address in the SDRAM that the output data will start from at the end of the next BOCF.
2. Load Delay parameters	<Delay Error Reg0> <Delay Error Reg1> <Delay Rate Reg0> <Delay Rate Reg1>	
3. Load Correlator Frame Header	<Correlator Frame Header RAM Bank A> for CFs 0,2,4,6,8,…. or <Correlator Frame Header RAM Bank B> for CFs 1,3,5,7,…	Correlator Frame header words are placed in alternating banks from addresses 0 -239. Each address is 16-bits wide and represents the a correlator frame header word.

To Stop Playback

1. Stop playback at the end of the current correlator frame.		Clear the suo_run bit in the <SU Output Configuration Register>. **Data output stops at the end of the current correlator frame, but BOCFs and RCLK continues.**

One can now either Restart or Resume playback as described in the Mark5B Specification.

To Restart Playback from a New Location

1. Go to **Configuration** General Setup		

To Resume Playback

1. Load SDRAM start address	<SDRAM Address0> <SDRAM Address1>	This is the address in the SDRAM that the output data will start from at the end of the next BOCF.
2. Load Delay parameters	<Delay Error Reg0> <Delay Error Reg1> <Delay Rate Reg0> <Delay Rate Reg1>	
3. Load Correlator Frame Header	<Correlator Frame Header RAM Bank A> for CFs 0,2,4,6,8,…. or <Correlator Frame Header RAM Bank B> for CFs 1,3,5,7,…	Correlator Frame header words are placed in alternating banks from addresses 0 -239.
3. Turn SU output on		Set the suo_run bit in the <SU Output Configuration Register>. **Output will begin on next BOCF.**