MARK 5 MEMO #055

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To: Mark 5 Development Group

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Subject: DOM VSI Operation

Initialization

Task	Parameters	Comments
1. Assert PLX reset to DOM.		
2. Turn interrupt propagation from PLX to CPU off.		Clear Interrupt control reg in I/O space. This won't be done once the interrupt handler is working.
3. Deassert PLX reset to DOM.		DOM is initialized to known state. All DOM blocks are disabled. No data flow.
4. Set VSI Mode.		Set VSI mode in <DOM Control Reg>. Clear vsio_run bit.

5. Setup RCLK		Set the internal clock to 32 MHz (not necessary for SU with a correlator but won't hurt) using <ICLK Control>.
		
		Set the appropriate configuration in the <RCLK PPS Rate Register> :
		rclk_rate_code = 000;
		PPS_div_code = 010 for 32
		MHz playback;
		If test mode (no correlator):
		use_internal_pps = 1
		If non-test (using correlator)
		use_internal_pps = 0
		After all that, clear the RCLK_TRISTATE_EN bit in the <DOM CONTROL REG>.
		Set the the mode field to SU in the same register.

6. Suppress PPSes		Set suppress_pps bit in the <System PPS Suppress Register>
7. Enable timing block.		Set the timing_en and bocf_gen_en bits in the <Enables Register>. **RCLK begins at output.**

8. Assert reset to all non-running, VSI relevant blocks.		In the <DOM Resets0> register set: fpdp_xface_rst, fpdp_fifo_rst, strip_header_rst, sh_fifo_rst, unpack_xbar_rst, xbar_ram_rst, cfdr_rst, delay_gen_rst, vsio_rst bits. In the <DOM Resets1> register set: sdram_xface_rst, fpdp_dcm_rst bits.
9. Tell StreamStor to start playing appropriate scan.		"play=off", "set_scan=?" , "play=on". This starts the FPDP clk but no data flows to the DOM because fpdp_xface_en is cleared.
10. Take the FPDP DCM out of reset now that the FPDP clk is going.		Clear fpdp_dcm_rst in <DOM Resets1>. Now the FPDP DCM can lock to the FPDP clock.
11. Wait 100 ms for DCM lock.		
12. Take all blocks out of reset.		Clear <DOM Reset0> and <DOM Reset1>.

Front End:

1. Configure DOM Front End.	<StreamStor Invalid Reg 0> <StreamStor Invalid Reg 1> <DIM Invalid Reg0> <DIM Invalid Reg1> <Disk Frames per Second> <Xbar Slice Setting RegN> (N=0:31) <Unpack Code Register>	This configures all blocks of the DOM before the RAM buffer. The blocks are not yet enabled. If Phase Cal is implemented, then phase increments are written here.
2. Configure Phase Cal/State Count		*If implemented, phase cal and state count are setup here.*

Back End:

1. Load Delay parameters	<Delay Error Reg0> <Delay Error Reg1> <Delay Rate Reg0> <Delay Rate Reg1>	These should all be set to 0

Initial values for output:

1. Load SDRAM start address	<SDRAM Address0> <SDRAM Address1>	This is the address in the SDRAM that the output data will start from at the end of the next BOCF.

Begin filling DOM buffers

1. Wait for SDRAM DCMs to finish locking.		Check Status Register bits DCM0 and DCM1 and sdram_clk_stopped. Make sure the DCM0 and DCM1 bits are ‘1’ and sdram_clk_stopped is ‘0’. This ensures that the SDRAM clocks work okay.
2. Turn VSI output off.		Clear vsio_run bit in the <VSI Output Configuration Reg>. This will keep data from flowing out of the DOM once blocks are enabled.
3. Turn phase cal interrupts on.		*If phase cal and state count are implemented, phase cal interrupts are turned on here. Phase Cal interrupts will be generated as soon as data begins to flow into the DOM and should be serviced throughout the scan.*
4. Enable relevant blocks in DOM		Enable fdpd_xface_en, strip_header_en, unpack_xbar_en, xbar_ram_en, sdram_arbiter_en, sdram_core_en, sdram_rcvr_en, delay_gen_en, vsio_en, timing_en (should already be set) **This will start data flowing into the DOM.**
5. Wait for SDRAM init/fill to finish.		Monitor sdram_init_done bit in <Status Register>

Begin VSI Output

1. Enable the ROT1PPS interrupt		Set the ROT1PPS_IM bit in the <DOM Interrupt Mask Register>
2. Wait for a ROT1PPS interrupt		
3. Turn VSI output on		Set the vsio_run bit in the <VSI Output Configuration Register>.
4. Unsupress a PPS.		Clear the suppress_pps bit in the <System PPS Suppress Register>
5. Wait for a ROT1PPS interrupt		**Output begins now.**
6. Supress PPSes.		Set the suppress_pps bit in the <System PPS Suppress Register>

While Running

When a data jump (delay shift) is required

1. Load SDRAM start address	<SDRAM Address0> <SDRAM Address1>	This is the address in the SDRAM that the output data will start from at the end of the next BOCF.
2. Unsupress a PPS.		Clear the suppress_pps bit in the <System PPS Suppress Register>
3. Wait for a ROT1PPS interrupt		**Output begins now.**
4. Supress PPSes.		Set the suppress_pps bit in the <System PPS Suppress Register>

To Stop Playback

1. Stop playback at the end of the current second.		Clear the vsio_run bit in the <VSI Output Configuration Register>. **Data output stops at the end of the current ROT second.**