## MARK 5 MEMO #071

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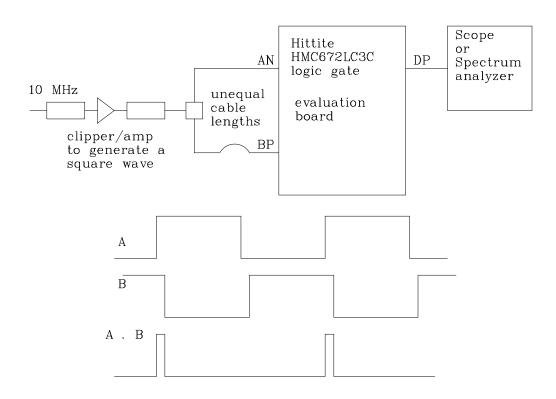
To: Mark 5 Development Group From: A.E.E. Rogers

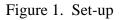
Subject: Test of Hittite logic gate

I ran tests of the Hittite logic gate HMC672LC3C evaluation board using an Agilent DCA-J86100C sampling scope and a spectrum analyzer. The set-up is shown in figure 1. When using the scope the input signal was a 640 MHz + 2 dBm sine wave followed by the diode chipper. When measuring the spectrum a 10 MHz signal was used with amplifier and diode clippers on both sides of the amplifier to get a sufficiently fast rise and fall time. To obtain an output rise time of 30 ps over 0.5 volts the input rise time has to be greater than 0.7 volts/ns because the gate has only 27 dB active gain.

Figure 2 shows the waveform of the gate output with cable lengths different by about 3 inches and figure 3 shows the waveform when the cable length difference is reduced to minimize the pulse width. The minimum pulse width that could be achieved was about 65 ps at the half voltage points which was considerably worse than the approximately 25 ps rise/fall time of the waveform of figure 2. Figure 4 shows the spectrum of the Hittite gate compared with the gated tunnel diode used in the VLBA calibrator (see VLBA acquisition memo #284, 7 Oct 91). Also shown is the spectrum from a single edge of an ADCMP572 comparator. Two different line differential delays are plotted. As the line lengths are made more equal the pulse width narrows up and the signal level drops. I was not able to get a smoothly decreasing response above about 9 GHz but the response up to 9 GHz is quite acceptable and if the pulse generator is to be used only up to 8.5 GHz the output level can be increased by increasing the line length difference. I experimented with changing VR (pin 14) but couldn't really improve the performance about 9 GHz.

All spectra are for a 10 MHz pulse repetition rate. From these results I suggest that the best approach given that tunnel diodes are no longer available, is to gate the output of the Hittite HMC672LC3C using a microwave switch. This will avoid the pulse width degradation which results from using the logic function. In addition a non-linear transmission line using variations could be used to further sharpen one edge of the square wave prior to the microwave switch as shown in the suggested block diagram or Figure 5.





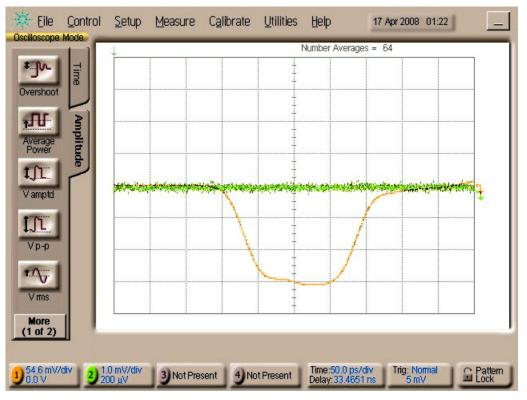


Figure 2. Output using AND gate to produce a narrow pulse as suggested by Tom Clark.

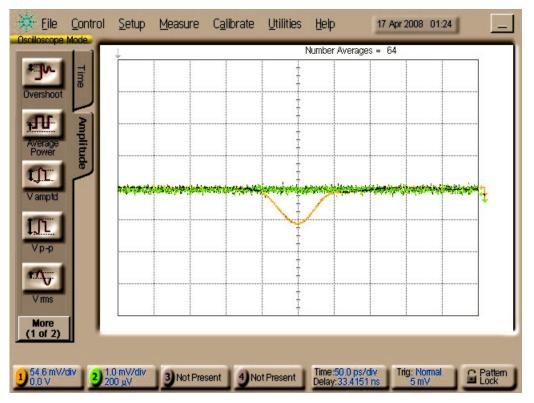


Figure 3. Narrowing down the difference in line length to minimize the pulse width.

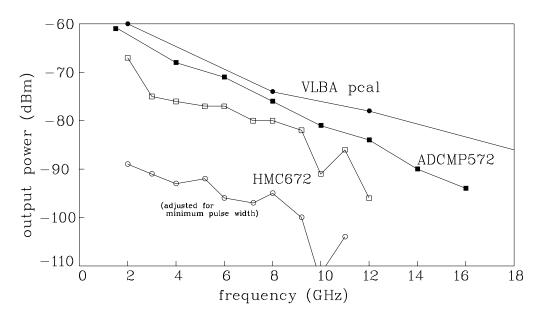


Figure 4. Spectra of various pulse generator configurations. Filled circles are values from VLBA memo on tunnel diode phase cal. Filled squares are from earlier test using a ADCMP572 comparator with latch enable function driven to lower the rise time on one edge of the square wave. Open circles and squares are for the HMC672 and two different line length differences. The lower curve corresponding to a path difference similar (but not quite the same) as in Figure 3.

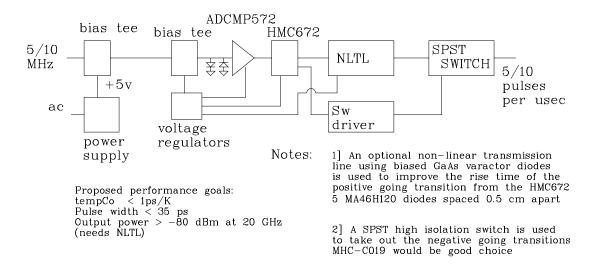


Figure 5. Suggested block diagram for improved performance.