MASSACHUSETTS INSTITUTE OF TECHNOLOGY

HAYSTACK OBSERVATORY

WESTFORD, MASSACHUSETTS 01886

Telephone: *978-692-4764*
Fax: *781-981-0590*

6 September 2005

TO: Dan Werthimer

FROM: Brian Fanous, Alan Whitney, Shep Doeleman, Hans Hinteregger, Alan Rogers

SUBJECT: Updated DBE specifications

This is an update of the memo dated 27 October 2005 attempting to specify the requirements for the VLBI DBE application. For reference purposes, a simplified block diagram is attached.

IF in:

#IFs: 2 (real)

IF BW: 512 MHz (0-512 MHz or 512-1024MHz)

Level: For the Atmel AT84AD001B sampler, full scale is ±0.25 volts

Sampling:

Rate: 1024 Ms/sec

Depth: 8 bits

Jitter: <10 psec rms with perfect external clock (desired for mm astronomy)

Aperture-delay temperature coefficient: <1 psec/degC (desired for geodesy)

External clock: 1024 MHz at 0dBm nominal

Operating modes:

Mode 1:

Divide IF1 into 32 16MHz channels; select channels 0-15 to VSI1, 16-31 to VSI2.
VSI clock rate is 32MHz; total aggregate data rate is 2048 Mbps.

Mode 2:

Divide IF1 into 32 16MHz channels; select channels 0-15 to VSI1.
Divide IF2 into 32 16MHz channels; select channels 0-15 to VSI2.
VSI clock rate is 32MHz; total aggregate data rate is 2048 Mbps.

Mode 3:

Divide IF1 into 16 32MHz channels; output to VSI1.
Divide IF2 into 16 32MHz channels; output to VSI2.
VSI clock rate is 64MHz; total aggregate data rate is 4096 Mbps.

Polyphase Filter Bank

We would like to have ~50-60dB rejection outside each frequency channel, but understand the achievable rejection may be limited by resources available on the FPGA.

VSI Output

Format: Each VSI output is 16 real channels of 2 bits/sample, with each channel occupying 2 adjacent VSI bit-streams.

Coding: We prefer to use the VLBA code, if possible, which is coded in offset binary. Going from most negative to most positive voltage sample, the code is SM=00,01,10,11. At the VSI output, the 'S' bit is placed on the even-numbered bit streams and the 'M' bit is placed on the odd-numbered bit streams.

1PPS tick:

See Figure 2. The system is synchronized to an external 1PPS pulse – EXT_1PPStick. This EXT_1PPStick is used to trigger an internally generated 1PPS – INT_1PPStick. The INT_1PPS is triggered by EXT_1PPStick but its period is controlled by clock division of the 1024 MHz sample clock. After INT_1PPStick generation begins EXT_1PPStick can be removed from the system as the entire system is now synched to INT_1PPStick. While some minimal (less than 1 microsecond) delay can exist between EXT_1PPStick and INT_1PPStick, it is crucial that INT_1PPStick have perfect periodicity (to the resolution of the sample clock – i.e. INT_1PPStick is asserted every 1024,000,000 sample clock cycles). The EXT_1PPStick is a TTL signal of arbitrary width, though at least 1 sample clock signal wide.

Which particular EXT_1PPStick to use to trigger the INT_1PPStick is determined by an ARM command sent to the serial port which will be sufficiently early to avoid a race condition (the ARM signal will be roughly ½ second before EXT_1PPStick is asserted).

INT_1PPStick is used to reset and synchronize the DSP signal chain and to mark the sample taken on the second tick (TOST). Every sample which enters the DBE input during INT_1PPStick assertion must be marked at the output by the VSI 1PPS tick assertion. This can be done via a counter or pipelining of the INT_1PPStick signal with enough delay stages to match the DSP signal chain pipeline delay from input to output.

VSI1PPS ticks at the VSI output must run continuously once the INT_1PPStick generation has begun.

Test Vector Generator (desired):

The VSI-defined TVG generates test-vector signals for verification of the DBE to Mark 5 interface; in accordance with the VSI specification, it resets on every VSI 1PPS tick and operates at the prevailing VSI clock rate. The TVG should be selectable dynamically to replace the normal data streams to the VSI1 and VSI2 outputs.

Electrical and timing: In accordance with VSI specification

Control

Operating mode selection:

It is desirable to be able to select the operating mode, to the extent possible, without opening the box or having to connect a JTAG interface. Perhaps several operating modes could be stored into a PROM, and the desired operating mode selected by DC control on some header pins, or via the serial interface.

1pps set

Some method must be devised to specify which external 1pps tick is to be used to synchronize the internal 1pps generator. One possibility is an 'arm' control applied sometime in the second previous to the desired external 1pps tick. The external 1pps is unnecessary and may be removed after synchronization. Refer to the above 1PPS description.

Channel gain:

The multi-bit output of each of the PFB channel must be multiplied by a coefficient determined from the state counts that are observed by the Mark 5B connected to the VSI outputs. This ensures the maximum SNR in the correlation results. The coefficient for each channel will, in general, be different to compensate for non-uniformity across the IF. The coefficients must be allowed to be changed dynamically, on a timescale of order a few seconds. What we envision is that a set of coefficients will be downloaded to the FPGA through the serial port, then a command will be issued (presumably also through the serial port) to put them into effect on the next 1PPS tick (or something like that). After the multiplication is done for each sample, only 2 bits will be retained – the sign bit and one threshold-amplitude bit (yet to be specified).

Timing Integrity

The timing integrity of the system must be such that the following rules are observed:

1. Once synchronized, the internal 1PPS generation is accountable solely to the 1024 MHz clock. There must be precisely 1024×10^6 sample clock cycles between each internal 1PPS tick.
2. The framing of the data within the PFB with respect to the internal 1PPS must be deterministic and reproducible, even through any reset or power cycling.
3. Assuming a perfect 1024MHz sample clock with no jitter, the sample jitter produced at the output of the A/D must not exceed 10 psec.

Test Vector Generator

The TVG should be selectable to replace output VSI data streams. The TVG is reset on each internal 1PPS tick. The TVG algorithm is detailed in the VSI-H specification, available at http://web.haystack.edu/vsi/index.html.

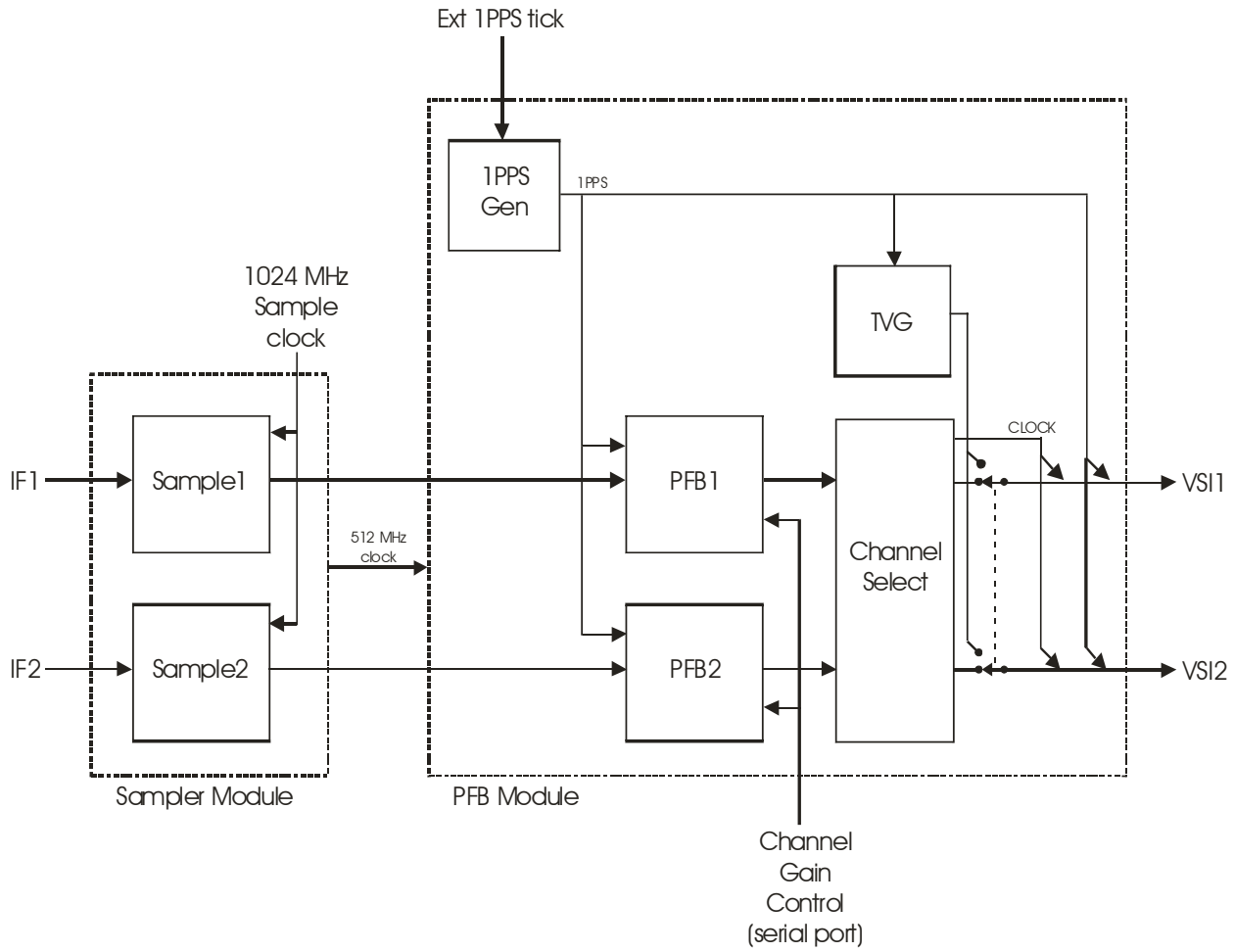

Figure 1: Simplified block diagram of proposed DBE

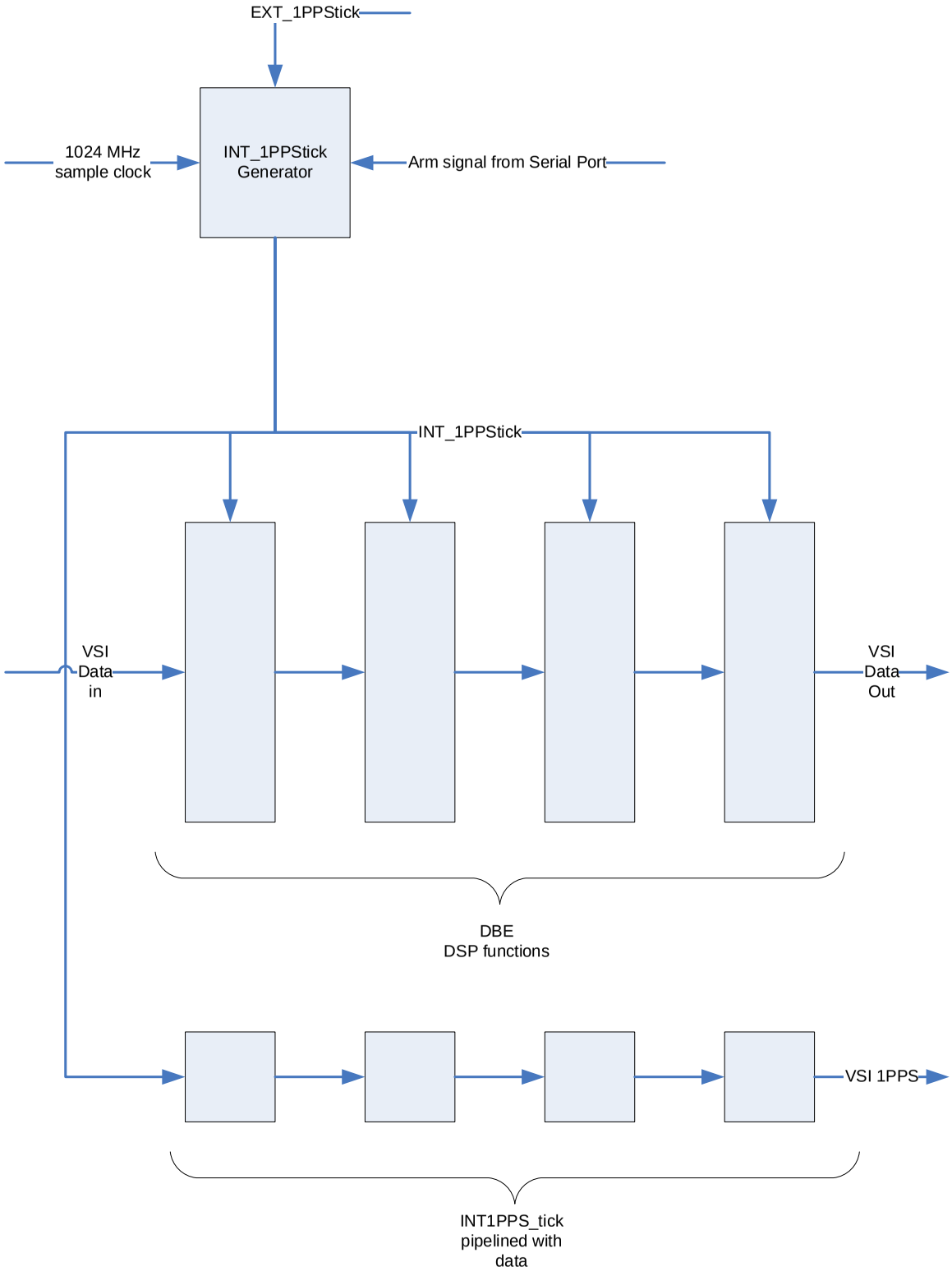

Figure 2 - 1PPS behavior