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TO: Dan Werthimer

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SUBJECT: Preliminary DBE specifications

This is a first cut at specification for the VLBI DBE that we have been discussing. For reference purposes, a simplified block diagram is attached.

IF in:

#IFs: 2 (real)

IF BW: 512 MHz (0-512 MHz or 512-1024MHz)

Level: For the Atmel AT84AD001B sampler, full scale is ±0.25 volts; typical operating input level should be ~8 mv rms (-29 dBm)

Sampling:

Rate: 1024 Ms/sec

Depth: 8 bits

Jitter: <1 psec rms with perfect external clock (desired for mm astronomy)

Aperture-delay temperature coefficient: <1 psec/degC (desired for geodesy)

External clock: 1024 MHz at 0dBm nominal

Operating modes:

Mode 1:

Divide IF1 into 32 16MHz channels; select channels 0-15 to VSI1, 16-31 to VSI2.
VSI clock rate is 32MHz; total aggregate data rate is 2048 Mbps.

Mode 2:

Divide IF1 into 32 16MHz channels; select channels 0-15 to VSI1.
Divide IF2 into 32 16MHz channels; select channels 0-15 to VSI2.
VSI clock rate is 32MHz; total aggregate data rate is 2048 Mbps.

Mode 3:

Divide IF1 into 16 32MHz channels; output to VSI1.
Divide IF2 into 16 32MHz channels; output to VSI2.
VSI clock rate is 64MHz; total aggregate data rate is 4096 Mbps.

VSI Output

Format: Each VSI output is 16 real channels of 2 bits/sample, with each channel occupying 2 adjacent VSI bit-streams.

Coding: We prefer to use the VLBA code, if possible, which is coded in offset binary. Going from most negative to most positive voltage sample, the code is SM=00,01,10,11. At the VSI output, the 'S' bit is placed on the even-numbered bit streams and the 'M' bit is placed on the odd-numbered bit streams.

1PPS tick:

A 1PPS signal that is derived by direct division of the sample clock will be generated on each VSI output connector. The epoch of the VSI 1PPS tick will be set once (and only once) from an external TTL 1PPS signal; after the initial setting, the external 1PPS signal may be removed with no effect on the VSI 1PPS tick.

Test Vector Generator (desired):

The VSI-defined TVG generates test-vector signals for verification of the DBE to Mark 5 interface; in accordance with the VSI specification, it resets on every VSI 1PPS tick and operates at the prevailing VSI clock rate. The TVG should be selectable dynamically to replace the normal data streams to the VSI1 and VSI2 outputs.

Electrical and timing: In accordance with VSI specification

Control

Operating mode selection:

It is desirable to be able to select the operating mode, to the extent possible, without opening the box or having to connect a JTAG interface. Perhaps several operating modes could be stored into a PROM, and the desired operating mode selected by DC control on some header pins, or via the serial interface.

1pps set

Some method must be devised to specify which external 1pps tick is to be used to start the internal 1pps generator. One possibility is an 'arm' control applied sometime in the second previous to the desired external 1pps tick.

Channel gain:

In order to ensure maximum SNR, the 'clipping' level (gain) of the sampled signal in each channel must be set near optimum. This is particularly important if the IF bandpass is not flat. As we discussed, the Mark 5B can measure state statistics and provide feedback to set the gain in each individual output channel. As you suggested, a serial interface can be provided to implement this gain control function.

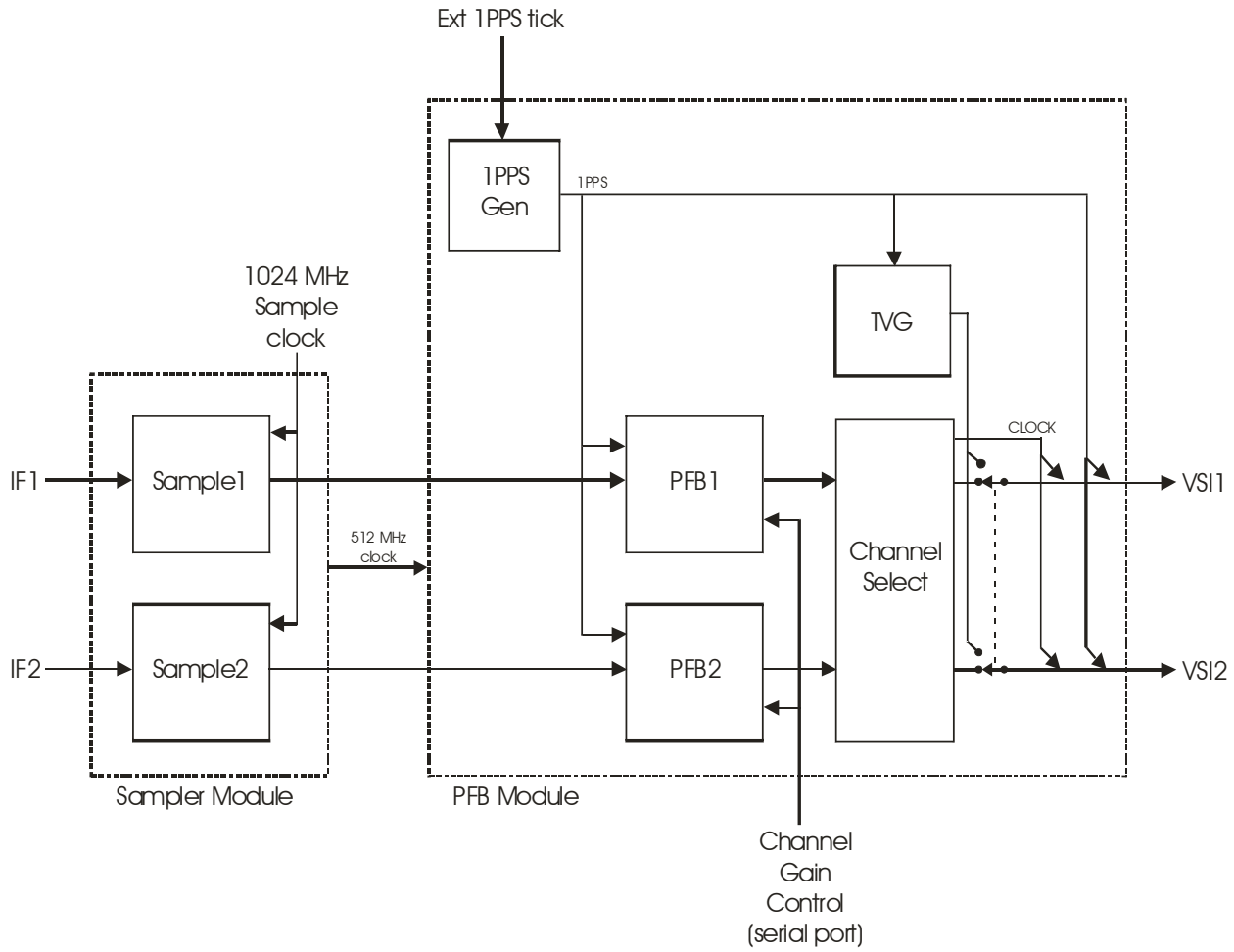

Figure 1: Simplified block diagram of proposed DBE