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To: UVLBI Group
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Subject: Current VLBI Application Block Diagram

The objective here is to outline the basic elements of the Haystack VLBI application effort using the ibob2 board and also start a memo series documenting this development effort. For the present time this memo focuses only on the application running internal to the FPGA and *not* the PowerPC (PPC) portion of the design. Only the interface External Bus Controller (EBC) to the PPC will be shown. A block diagram of the major modules that together make up the VLBI instrument is presented with a brief description of the blocks. Details of the connections (interfaces) will be made available as the modules progress through the design cycle. Typically the high speed data flow connections between the modules will be data, clock, data valid and reset. There will also be connections between modules and the PPC through memory mapped registers for module configuration and status information. These modules can and should be further broken down to a more detailed level as the design progresses.

The first VLBI design will be based on the Haystack/Berkeley VLBI implementation, which was implemented on the original ibob hardware. This will serve a two fold purpose; first, the output of the new ibob2 VLBI instrument can be directly compared to a “known to be working” ibob design, Secondly, the working modules can be used as a basis for expanding the design to higher bandwidths, higher channel counts, etc.

1. 1PPS Arming Module - This module is responsible for synchronizing the internal processes to the external 1pps and generating the internal 1pps clock.
2. 1PPS Data Synchronization Timing Module – This module is responsible for time tagging the data packets according to the Mark5C Specification.
3. ADC Module – This is the interface between the ADC board and the FPGA. It will configure the ADC, clock data into the FPGA for further processing.
4. IF Power Estimator – Used to estimate the input power of the given IF in order to manually apply feedback control signal to an AGC via a Graphical User Interface (GUI).
5. AGC External Interface – Interface to an external AGC module (TBD). Most probably a serial data interface device that will be driven from ibob2 IO lines.

6. N-Channel Polyphase Filter Bank – The first implementation of the PFB will be a 32 Mz design in order to have a direct replacement for the current ibob design. Next will be a 16MHz version and then future designs will be focus on increasing channel count, bandwidth, etc.
7. N-Channel 2 bit Quantizer – Sets the quantization threshold.
8. N-Channel Threshold Estimator & Statistics – Calculates the quantization threshold based on sampled statistics per channel. Channel statistics and threshold settings will be available via the GUI.
9. Test Vector Generator – Used to inject test vectors into the high speed data link (10Gbe).
10. Corner Turner – Used to group processed data into frequency channels for transmission over 10Gbe.
11. 10Gbe – High speed data transmission interface.

