VSRT MEMO #016

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To: VSRT Group
From: Alan E.E. Rogers
Subject: Frame grabber configuration

1] Configuration of the SAA7113H chip in the video frame grabber.
The analog processor, ADC and output format in the SAA7113H is programmed via an I^2C – bus which can be accessed via address 0×4a in the EM2820. The following configuration was used

Sub-address	(Hex)	Function	Value	(Hex)
00		Chip version Read only	14	
01		Increment delay	08	
02		Analog 1 input	C0	
	11	Amplifier with anti-alias filter		
	00	No ADC hysteisis		
	0000	Mode 0 chroma and luma from pin 4		
03		Fixed gain, white peak off	77	*
04		Gain ff	ff	*
05		Gain ff	ff	*
06			E9	
07			0D	
08	AUFD=0; 60Hz525; HPLL=0(fixed horizontal line freq)		5C	*
09	BYPS=1; APER=0		80	*
0A			80	
0B			47	
0C			40	
0D			00	
0E			01	

0F		ACGC =1 = programmable gain	80	*
10			00	
11			OC	
12			01	
13→3F			00	
40			02	
41→57			FF	
58			00	
59			54	
5A			07	
5B			83	
5C→5F			00	

Non standard values (i.e. values which are different from those given in table 74 of data sheet are indicated with * in the last column).

The sample rate is 1/27 MHz which is reduced by a factor of 8 in the output mode of the em2820. A horizontal line in the em2820 output is 180 samples or 53.333 microseconds. A complete TV line in the 60Hz, 525 line mode is 63.5566 microseconds (15734 Hz line frequency) so 34.5 "blank" samples need to be added to account for the horizontal blanking. I have searched for a way of avoiding the 16% loss of data samples without success.

2] EM2820 configuration

EM2820 registers

Register	Address (Hex)	Value (Hex)	
CHIPID-REG	0a	Read only	
YGAIN_REG	20	10	*
YOFFSET_REG	21	00	Adds to output
UVGAIN_REG	22	10	No effect
UOFFSET_REG	23	00	
VOFFSET_REG	24	00	
SHARPNESS_REG	26	00	No effect
GAMMA_REG	14	20	No effect
RGAIN_REG	15	20	
GGAIN_REG	16	20	
BGAIN_REG	17	20	
ROFFSET_REG	18	00	
GOFFSET_REG	19	00	
BOFFSET_REG	1a	00	No effect
OFLOW_REG	1b	00	*
HSTART_REG	1C	00	
CWIDTH_REG	0E	B4	*

CHEIGHT_REG	1F	02	*
XMIN_REG	28	00	
XMAX_REG	29	FF	
YMIN_REG	2A	00	
YMAX_REG	2B	FF	
HSCALELOW_REG	30	00	
HSCALEHIGH_REG	31	10	*
VSCALELOW_REG	32	00	
VSCALEHIGH_REG	33	00	
OUTFMT_REG	27	30	*
VINMODE_REG	10	10	
VINCTRL_REG	11	11	*
COMPR_REG	26	30	*
USBSUSP_REG	0C		*
VINENABLE_REG	12	67	*

OUTFMT_REG	0011	0000	drops sample rate by 2
HSCALEHIGH_REG	10		
	20		drops # samples per line
COMP_REG	00110000		drops sample rate by 4
VINENABLE_REG	0110 0111		starts
	0010 0111		stops
USB_SUSP_REG	bit 0×10		sets/checks suspended USB
CHEIGHT_REG			sets the number of lines returned
	2	returns 2888 bytes = 8 lines of 180 samples	
	4	returns 5768 bytes = 16 lines of 180 samples	
	8	returns 11528 bytes = 32 lines of 180 samples	

The USB has to keep up with the capture in all cases except 8 lines which is small enough to fit in the em2820 buffer. The sync (with value 0×5A) should be at the start of the data.

Registers marked with * are required, others may not be needed.

A good reference is /usr/scr/linux_2.6_gentoo_r1/drivers/media/video/em28xx.