VLBI Digital Backend Program

Sheperd Doeleman
Haystack Observatory
Motivation for wideband DBE

• VLBI data rates up by only x4 since 1980’s.
• Modern FPGAs give increased performance at small fractions of Mark4/VLBA cost.
• For continuum obs. widebanding highly cost effective vs. larger dishes: going from 512Mb/s to 4Gb/s same as 42m VLBA dishes.
• DBE systems are portable.
• Wideband obs. particularly important for class of phase ref., high frequency, fast frequency switching projects.
• Industry driven growth path.
Proposal History

• Fall 2004: initial collaboration between Berkeley SSL and Haystack on DBE.
  – SSL Hardware: ADC, iBOB, BEE2
  – iBOB (single FPGA) able to meet DBE specs.
  – Algorithm work on DSP necessary for VLBI.
  – Haystack contributes to hardware/firmware work at SSL.

• Jan 2005: DBE proposal submitted to NSF.

• Apr 2006: DBE grant received.
Prototype DBE Architecture
Prototype DBE Modes

- **Mode 1:** 512MHz BW input, PFB to 32 channels each 16MHz and 2-bit, output 16 channels to VSI: 1Gb/s.
- **Mode 2:** mode 1, but remaining 16 channels output to second VSI connector: 2Gb/s.
- **Mode 3:** 512MHz BW input, PFB to 16 channels each 32MHz and 2-bit, output all channels to VSI: 2Gb/s.
Tests with DBE Prototypes

- Running in Mode 3 with Mark5b bitmask to record only sign bits (1Gb/s).
- Zero baseline tests w/o and w/ rate offset.
- 230GHz VLBI between SMTO-SMA/CSO.
- X-band obs. between Westford-GGAO.
  - successful test with simultaneous Mark4/Mark5A and DBE/Mark5B recordings.
  - Excellent agreement between Mark4 and DBE fringes.
  - SBD and MBD for DBE fringes agree to within ambiguity: consequence of PFB.
- Field system running on Mark5B, channel gains set manually via serial link from Mark5B to DBE.
DBE X-band Fringes
Near Term Plans

• Firmware:
  – Double-duty FFT to process two 512MHz IFs on single iBOB/ADC pair (daughter VSI board); single iBOB requires 2 Mark5B+ recorders for 4Gb/s aggregate rate.
  – Implement channel selector and VSI input on iBOB for Geodetic bandwidth synthesis.
  – Implement 16MHz channel modes.

• Hardware:
  – Complete dual iBOB chassis for Geodetic/Astronomy applications.
Proposed DBE System for Geodesy and Astronomy Applications.

COST for 2-IFs:
- iADC/iBOB = $3.2K
- Samp Clk = $150
- Chassis = $1K
- Total = $4.35K in parts.
2.5 Year Plans

- **Firmware:**
  - State Count level correction on-board DBE; possibly done on Mark5B with serial feedback.
  - Optimize Filter shapes (increase FIR/Interpolator taps).
  - 10GigE protocol and output for compatibility with commercial NICs: COTS storage.
  - Pulsar gating capability.
  - Digital Downconverter implementation for spectral line applications.

- **Hardware:**
  - IF processing front end: input is 100MHz to 15GHz IF, output is filtered 512MHz band. ($7.5-10K)
  - Decision on re-spin of iBOB for VLBI-specific application: NRAO collaboration?
  - Final Chassis build.

- **Software:**
  - Control software integration.
  - Solution to DBE mode switching.
Effects of filter taps

FIR: 8
Interp: 16
Loss=1.3%

FIR: 16
Interp: 16
Loss=0.5%
Future

• SSL has 3 year ATI grant to continue general purpose FPGA development for Radio Astronomy.
• Virtex 5 based hardware within 3 years with corresponding firmware libraries.
• ADC will have 3GSamp/sec AD with 6GSamp/sec interleave mode.
• Haystack Burst Mode proposal submitted yesterday: 16Gb/s bursts from 2 DBEs, stored in RAM, read out to COTS SATA RAID.
Burst Mode

4 x 500MHz IF

Station 1PPS

H-maser 5/10MHz

4 x 500MHz IF

DBE

4Gbps bursts
10GigE
4Gbps bursts
10GigE

Buffer PC

10GgigE NIC
32GB RAM

Buffer PC

10GgigE NIC
32GB RAM

Control PC

Pulsar-gating control

Control

Completely COTS

100MBps SATA2

4-disk SATA RAID

100MBps SATA2

4-disk SATA RAID

10GgigE NIC

10GgigE NIC

4Gbps bursts
10GigE

32GB

32GB

4Gbps

100MBps

SATA2

SATA2

PC

4Gbps bursts

32GB

4Gbps bursts

100MBps

SATA2

SATA2

10GgigE NIC

10GgigE NIC

5/10MHz

Buffer PC

Control

Completely COTS

Buffer PC

Control

Completely COTS

Buffer PC

Control