EVN dBBC

from

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DBBC General Features

- Four IFs Input in the range 10-512 or 512-1024 MHz
- Four Ifs bands available for a single group of output data channel selection
- 1.024 GHz fixed frequency sampling clock
- Channel bandwidth ranging between 500KHz to 16 MHz (prel.)
- Tuning step 50 KHz (prel.)
- Multiple architecture using fully re-configurable FPGA Core Modules
- Modular realization for cascaded processing
- Field System support
DBBC General Features (cont.)

• Data out as single or double VSI interface
• Total power measurement capability
• Continuous Tsys measurement capability
• Autocorrelation function for improving band shape
• Pseudo noise and notes injection
• Digital to analog converter monitor output
• Digital AGC
• Optional gigabit data transfer
DBBC Status

• Prototype demonstrated at 32 MHz channel BW (on one end of baseline)
• Single-channel dBBC boards being upgraded (newer Xilinx) to support four dBBC channels per board
• Updated prototype expected complete end 2007
• VSI↔10GigE conversion board under development
• Expected cost ~40K Euros for 16-channel system
• Recent dBBC CDR gave go-ahead for continued development
• Being jointly developed by CNR/MPI
The first CoreBoard is performing RFI active mitigation.
4 ADBoard + 8 CoreModule Stack
DBBC – Backend
The End