**TO:** Mark 5B design group  
**FROM:** R. Cappallo, A. Whitney  
**SUBJECT:** Mark 5B status LED’s – functions and layout

8 tri-colored LED’s are suggested, with the following functions:

<table>
<thead>
<tr>
<th>Label</th>
<th>Meaning</th>
<th>DIM mode</th>
<th>DOM mode</th>
</tr>
</thead>
</table>
| MOD   | Operating mode | G – DIM  
B – DOM/SU  
R – DOM/VSI  
Off – FPGA programming failure |  |
| PPS   | 1PPS | Flash at 1PPS rate:  
R - Not sync’ed; flashes with selected external 1PPS  
G - Sync’ed: flash with DOT1PPS  
Not flashing – no clock | Flash G with DSP1PPS |
| VAL   | Data validity | G – ‘valid’ data at DIM input  
B – TVG selected and active  
R – ‘invalid’ data at DIM input | G – ‘valid’ data at DOM output  
B – TVR active; TVG data recognized  
R – ‘invalid’ data at DOM output |
| FLO   | FPDP data flow | G – writing valid data to FPDP  
R – writing fill pattern  
Off – no data flow | G – reading valid data from FPDP  
R – reading fill pattern  
Off – no data flow |
| ERR   | Error | G – normal operation  
R - Internal error detected |  |
| TVR   | Delay buffer state | G – TVR active  
R – TVR error detected | G – write in 2nd quadrant behind read  
B – write in 3rd quadrant behind read  
R – write in 1st quadrant behind read  
Off – write in 4th quadrant behind read |
| SW1   | Software controlled | - | - |
| SW2   | Software controlled | - | - |

Key:  
G – green  
R – red  
B – blue