DBBC3
DEVELOPMENT OF A 32 GBPS DIGITAL BACKEND

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Partner:

INAF – Italy

MPIfR - Germany

OSO – Sweden

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Background

- Astronomic VLBI requires improvement in the overall sensitivity (4Gbps EVN, mmVLBI, 32Gbps EVN)
- Geodetic VLBI requires improvement in delay determination (VLBI2010)
- Current state of the art technologies offers every day new opportunities
- Two generation of the DBBC system represent a reasonable starting platform to develop a higher data rate backend
**DBBC Evolution**

**DBBC1** 2004 - 2008
  in: 4 x IF-512MHz
  out: **DDC** 16xbbc(1-2-4-8-16MHz)@32MHz
      0.512/1.024Gbps

**DBBC2** 2007 – to date
  in: 4 x IF-512/1024MHz
  out: **DDC** 16xbbc(1-2-4-8-16MHz)@32MHz
      **PFB** 4 x 16 x 32MHz@64MHz
      4.096/8.192Gbps

**DBBC2010** 2009 – to date
  in: 8 x IF – 512/1024MHz
  out: **PFB** / **DSC** 16.384/32.768Gbps
DBBC3 General Performance for EVN

- Number of Input IF: 1 - 4
- Instantaneous bandwidth ea. RF: \( \geq 4 \text{ GHz} \)
- Sampling representation: 8-10 bit
- Processing capability: able to support wide band DDC, PFB, DSC and more (pulsar, polarimetry, spectroscopy, holography, etc.)
- Output: VDIF Ethernet packets, \( \geq 32 \text{Gbps} \)
- Compatibility with the existing DBBC environment
DBBC3 Architecture for EVN

**ADB3-L**
- 10 bit Sampler
- 10 bit Sampler
- Synthesizer

**CORE3-L**
- DDC PFB DSC
- DDC PFB DSC
- Management

**FILA40G**
- PACKETS HANDLING
- BUFFER
- 40G
- Management

- 2 x 81.920 Gbps
- 2 x 4 GHz bwd
- 4 x 10 GE
- 1 x 40 GE
- 32 Gbps as 4 x 8 Gbps
- (128 Gbps as 16 x 8 Gbps ready)
- 32 Gbps

40/100G network to buffer cloud / correlator
ADB3-L General Performance

- **ADB3-L:**
  - Number of IFs: 2
  - Equivalent Sample Rate ea. IF: 8.192 GSps
  - Instantaneous bandwidth ea. IF: 4 GHz
  - Internal Sampling representation ea.: 10 bit

- Real/Complex Sampling

- Compatibility with the existing DBBC environment
### ADB3-L Sampler

- **Sampling Clock Generation**
  - 10 MHz
  - 1 PPS

- **Samplers**
  - **Sampler 1**
    - 1 x 4 GHz
  - **Sampler 2**
    - 1 x 4 GHz

- **Serial Link TX**
  - 8 x 10 Gbps

- **ADB3-H Adapters**
  - 4 x 1 GHz

- **Connections**
  - 8 x 10 Gbps
  - 4 x 1 GHz
CORE3-L General Performance

Core3-L

Number of Input: max 16 serial links 10Gbps
Number of Output: max 16 serial links 10Gbps
Input Sampling Representation: 8 -10 bit
Processing capability: DDC, PFB, DCS
Output: VDIF Ethernet packets, >=32Gbps
Compatibility with the existing DBBC environment
CORE3-L

Max
16 x 10Gbps

4 x 12.5Gbps

Serial Link RX

HSI

PROCESSING UNIT

Serial Link TX

HSO

Max
16 x 10Gbps

4 x 12.5Gbps

Pass-band

-100 dB

CCM
DBBC3 Architecture for VLBI2010

Wide Band
VLBI2010 Rx

Receiver IF
Left/Right
2 x 14 GHz bwd
2 x 224 Gbps

ADER3-H

8 bit Sampler
8 bit Sampler
Synthesizer

CORE3-H

DDC PFB DSC
DDC PFB DSC
Management

ADB3-L replacement

ADER3-H adapter
ADER3-H adapter
Synthesizer

CORE3-L

DDC PFB DSC
DDC PFB DSC
Management

 реализация этой функции

FILA40G

PACKETS HANDLING BUFFER 40G
Management

10/40/100G network to buffer cloud / correlator

64 Gbps as 8 x 8 Gbps
384 Gbps as 48 x 8 Gbps ready

32 Gbps as 4 x 8 Gbps
(128 Gbps as 16 x 8 Gbps ready)

32 Gbps

DBBC2010 performs this functionality
DBBC3 Architecture for VLBI2010

Wide Band VLBI2010 Rx
- Receiver IF Left/Right
- 2 x 14 GHz bwd

ADB3-H
- 8 bit Sampler
- Synthesizer

CORE3-H
- DDC PFB DSC
- Management

FILA40G
- Receiver Digital IF Left/Right
- 64 Gbps as 8 x 8 Gbps
- 384 Gbps as 48 x 8 Gbps ready

DBBC2010
- ADB3-H adapter
- 8 x 1 GHz bwd

4 x 10 GE
- 32 Gbps as 4 x 8 Gbps

1 x 40 GE
- 32 Gbps
ADB3-H General Performance

- **ADB3-H:**
  - Number of IFs: 4
  - Equivalent Sample Rate ea. IF: 28.672 GSps
  - Instantaneous bandwidth ea. IF: 14.336 GHz
  - Sampling representation: 8 bit (ENOB 5.8 - 6.5 bit)

- Real/Complex Sampling
- Compatibility with existing DBBC environment
ADB3-H Sampler

10 MHz
1 PPS

14 GHz
Sampling Clock Generation

14 GHz
Sampler 1

14 GHz
Sampler 2

14 GHz
Sampler 3

14 GHz
Sampler 4

Serial Link TX

24 x 11.2 Gbps

24 x 11.2 Gbps

24 x 11.2 Gbps

24x 11.2 Gbps
CORE3-H General Performance

- Core3-H
- Number of Input: max 48 serial links 11.2Gbps
- Number of Output: max 48 serial links 11.2Gbps
- Input Sampling Representation: 8-10 bit
- Processing capability: WB*-DDC, WB*-PFB, WB*-DCS
- Output: VDIF Ethernet packets, >=32Gbps
- Compatibility with existing DBBC environment

* Wide band
CORE3-H

Serial Link RX

HSI

PROCESSING UNIT
3 TMACS

HSO

Serial Link TX

Max
48 x 11.2Gbps

8 x 12.5Gbps

Max
48 x 11.2Gbps

8 x 12.5Gbps

Pass-band

-100 dB
FILA40G Single Module General Performance

- Serial Link Input:  = 4 x 10Gbps
- Serial Link Processed Output:  = 4 x 10Gbps
- Serial Link Output:  = 1 x 40Gbps
- Packets manipulating capability (filtering, pulsar gating, burst mode, etc.)
- Packets forwarding capability (different correlator nodes, different correlator sites, etc.)
- Packets large buffering (RAM/HD/SSD)
- Packets monitoring capability
FILA40 Architecture
Single Module

- Large Area Buffer
- 40G Packet Forwarding Engine
- User interaction and monitoring
- Packet Management
- 1 x 40 Gbps
- 4 x 10 Gbps
- 4 lambda transceiver
- GLASS
Some ADB3-H preliminary measurements

DIVA Kickoff - Bonn, May 8th 2012
5 GHz single tone
10 GHz single tone
12 GHz single tone
14 GHz single tone
16 GHz single tone
Some ADB3-H preliminary measurements
Full 14GHz band cross-correlation
Single 14GHz tone cross-correlation
Thank you