JPL/DSN

DSCC VLBI PROCESSOR

DVP

DEVELOPMENT STATUS

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**DVP IMPLEMENTATION STATUS**

**July 2013 target operational date**

- Madrid DVP in place and being assembled
- Goldstone DVP in transit
  - Fringe Test to Madrid when installed
- Canberra DVP on hold at JPL for hardware verification
  - VRTM Board remanufacture in process
- DSS-13 DVP used as SW development platform
HARDWARE ASSEMBLIES

12x2 JFW MATRIX SWITCH
50 – 1000 MHz

IF DIGITIZER (IFD)
Separate Enclosure,
Good Analog/Digital
Isolation to avoid
spurs
HARDWARE ASSEMBLIES

VRTM AND ROACH ASSEMBLY
VRTM Converts fiber from IFD to copper for ROACH

MARK5C

DVP M&C HOST
Dell Computer Running Debian Linux
Mark5C SOFTWARE

- Conduant SDK 9.2
- JPL-developed Record and Monitor Suite
  - 2Gb/s Achieved Consistently
- SSReset and SS Erase
- fuseMk5 for Scan File Access
- VDIF Data Format Only
  - All Channels in each packet
Inputs and Outputs

- VEX Schedule File
- Antenna Pointing file
- Station Briefing Message
- Mark5 Disk Module
- PCFS-Style Log File
  - PCFS-style monitor data
    - WX, Mark5C, Phase-cal, Antenna Status, GPS, etc.
Questions?