Uniboard based digital receiver

G. Comoretto$^1$, A. Russo$^1$, G. Knittel$^2$

1- INAF Osservatorio di Arcetri
2- MPIfR – Bonn
Plus many others at Jive, Astron, Bordeaux, Bonn
Not really VLBI
Pulsar timing: why
Pulsar machine architecture
GPU signal processing
The Uniboard
Hybrid architecture (polyphase + DBBC) for a digital receiver, the best of both words
How to design large filters without Hanning windows
How many bits are enough? Nonlinearity and Gaussian noise
Back to VLBI
Uniboard based digital receiver

- Not VLBI, but close to a VLBI digital receiver
- Scientific rationale: Precision binary pulsar timing for General Relativity tests

*FP7 “Beacon in the dark” (MPiF)*

- Strong Equivalence Principle
- Scalar-tensor gravity theories
- PPN parameters
- Low frequency gravitational waves
- Equation of state for dense matters
Uniboard based digital receiver

- Wideband pulsar receiver
  - 2 x 3.125 GHz rec. BW
  - 2x1.5 GHz usable BW
  - 144 dBBC bank
- GPU based processor
  - 16 dual core ATI GPUs
Processing

Antenna, vertical Polarization
1. Analog/Digital Conversion
   2. Filterbank
   3. FFT
   4. Dedispersion
   5. Inverse FFT
   7. Folding
   8. Archive

Antenna, horizontal Polarization
1. Analog/Digital Conversion
   2. Filterbank
   3. FFT
   4. Dedispersion
   5. Inverse FFT

Typically 8 bits per Sample
Set of ~30MHz-Subbands On 4M complex Samples per Subband 4M complex Multiplies

②: Interface between the blocks is 10Gb Ethernet
Pulsar timing on a GPU

1 of 4 processing computers

4 x Radeon HD6990
8 GPUs

Tyan B7015 Chassis

2 Dual-Port 10GbE Cards (not shown)
GPU processing pipeline

- Minimize memory transfers
- Ethernet card writes data directly in user space memory
- Processing done mostly on local processor memory and local data storage
- Programming in GPU assembler
Preliminary GPU software results

Comparison of pipeline results for PSR1937+21
- Top: processing on GPU
- Bottom: processing on normal CPU

- Hard to compare to other solutions
- DSPSR: 512MHz on 4 WS, 4 Nvidia Tesla C2050
- CASPSR: 400MHz on 4 WS, 8 Nvidia Tesla C1060
- Nancay: 400MHz on 4 WS, 8 Nvidia GTX 280
- own: 300MHz, 1 WS, 1 AMD HD6990
Uniboard

- FP7 Radionet project - JIVE
- General purpose board
  - 4+4 FPGAS (Stratix4)
  - 1288 18 bit multipliers
  - 14 Mbit block memory
  - 16 x 4GB DDR3 banks
  - 16 +16 10G links
  - Internal 1Gbit Ethernet
  - Mesh of 4x4 6.4 Gb links

LVDS inputs & CX4 10GBE

10 GBE SFP+

Back nodes
Front nodes
Digital receiver architecture

- Input: 2x 6250 MS/s 8 bit ADC
- Dual stage filtering
  - 1\textsuperscript{st} stage: polyphase filterbank, ½ Nyquist spacing, 32 channels
  - 2\textsuperscript{nd} stage: array of fixed band dBBCs, 1/8 band, 87% usable BW
- Output: 2 x 72 complex signals, 24.4 MS/s 8 bit, over 12x10GBE
Digital receiver architecture

- Back nodes: 2 nodes x polarization
  - LVDS line receivers,
  - Polyphase filter + first 5 FFT stages

- Front nodes (each of 4)
  - Last FFT stage: 6 x 160 MHz BW, 195 MS/s, 60 MHz overlap
  - 18 BBC x 2 pol: 21.4 MHz BW, 24.4 MS/s,
  - Formatter and packetized for UDP 10G link (3 links x node)
- Discontinuous input band
- No "holes"
- Minimize discarded regions (overlap)
- Covered by 18 polyphase filter channels, and by 70 DBBCs: 1495 MHz
- No processing of unused spectral regions
- Large FIR filter: 1024 taps
- Equiripple response desired
  - Design scaled filter
  - Extend in frequency domain
  - Fit key (extreme) coefficients
- > 95 dB stopband, 0.005 dB ripple (0.1% p-p)
- 83% usable BW (33% overlap)
Filter design - dBBC

- Initial filter: 84.4% (27/32) BW
- Request: 1/8 band tuning step
- Final filter: 87.5% (28/32)
- In-band ripple rises: 0.05 dB → 0.4 dB (10% p-p)
- Needs passband correction
Quantization issues

- Need to perform multiple requantizations
- Nondeterministic (noise) signals
- Effect on linearity and dynamic range poorly studied

**Method**

"Van Vleck" analysis for bivariate Gaussian noise with many bit quantization

**Results:**

- No appreciable SNR degradation even with just 8 bit
- Signal RMS amplitude must not exceed 10-12% of total representation range
- Minimum RMS amplitude: 4-5% of range for 8 bit

RMS optimal amplitude:
- 12-25 ADC units for 8 bit quantization
- 14-45 ADC units for 9 bit quantization
Quantization issues

Truncation in FFT
- Effects studied by numeric simulations
  - Signal: deterministic PRGN + monochromatic line
- 18 bit truncation between FFT stages:
  - Rejection ~90 dB
- 8 bit truncation in one FFT stage (with gain adjustment)
  - Rejection ~70 dB
- Final solution: 12 bit, as only 48 polyphase filter channels transmitted to FN
  - Negligible rejection degradation
Resources usage

- Back node:
  - 922 multipliers (72%)
  - 2.4 Mbit (16%)
  - 43K (24%) of logic elements

- Front node
  - 1272 multipliers (99%)
  - 1.6 Mbit (11%)
  - 96K (53%) of logic elements
Simulation results

- Functional testing: step frequency sinewave
- No dithering: worse than real situation
- > 60 dB SFDR
Project status

- ADC board
- Interposer board:
  - PCB design
  - Assembly and testing
- GPU software

- FPGA Design:
  - Design
  - Functional simulation
  - Implementation
  - Functional on-board test
  - Integration with ADC
  - Control software

Sweeping tone test using Modelsim
VLBI applications

- Same structure of a VLBI dbbc
- Library of general purpose modules
  - BBC, VDIF formatter, spectrometer
  - (mostly) architecture independent
- 64x64MHz BBCs: 16 Gbps *tunable* system on a board

**Variable decimation BBC**
- Decimation from $\frac{1}{2}$ to $\frac{1}{256}$
- Bandshape scales with decimation
- Real or complex output
- 80 dB stopband, 0.003 dB ripple

**VDIF/UDP/ETH10G interface**
- 16 channels/link
- Each channel has independent
  - destination addr/port
  - bandwidth, format, packet length
- Scheduler sends 1st ready packet
Conclusions

- Hybrid architecture (polyphase + tunable BBC): wideband and tunable
- Wideband (6.25 GHz) system with 140 dBBC on a single board
- 1.6 GHz BW – 32 BBC system possible on a single FPGA
- Future work: 8 GHz 64-128 BBC system on one board (32Gbps)

*Uniboard as powerful testbench for large systems*

Thank you