# CDAS2: Ready for VGOS and Deep Space Exploration

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## 1 Introduction

After several years of work, CDAS2 has been grown up step by step. Different set of firmware and software on the same hardware platform provide different devices, CDAS2-PFB for VGOS and CDAS2-DDC for deep space exploration. Before the end of this year, CDAS2-DDC will be implemented in CVN stations. And CDAS2-PFB also will be implemented in the VGOS station after it is established.

## 2 The hardware for CDAS2

CDAS2 has been settled in a 1U chassis with two boards. On the board which installed LEDs, there is a clock synthesizer and two pre-amplifiers. The synthesizer can generate sampling clock such as 1024MHz from 10MHz clock source. Each pre-amplifiers has 30dB gain that can provide suitable power level for ADC. On the other board which installed SPF+ and RJ45 connecters, there is a dual channels ADC and a FPGA on the other board. Fig.1 shows two working CDAS2s on the rack.

Fig.1 CDAS2 hardware

CDAS2 hardware characters:

- 2 IF@512MHz BW inputs
- 30dB gain for each pre-amplifier
- Sampling clock synthesizer
- 1 Xilinx Kintex7 for data process
- 2 SPF+ for TenGiga Ethernet

## 3 The common features

Although the algorithms for CDAS2-PFB and CDAS2-DDC are different, many other features are same such as time synchronization, power calculation, data snapshot, parameters setting and system update. These features will make the device more convenient to use and maintenance.

The features including:

- Formatter time can be synchronized with NTP or RTC
- Compatible with MK5B and VDIF
- Full-band(512MHz) power calculation
- Sub-channel power calculation
- PPS status monitor
- Temperature and voltage monitor
- Realtime data snapshot
- Remote system update

## 4 CDAS2-PFB

For VGOS application, since the LO of UDC is tunable, the digital backend only need to divide the IF band equally. Usually we divided 512MHz bandwidth into 16 channels with PFB algorithm. And each channel is 32MHz band, as Fig.4(a) shows. Actually, we have got the band divided as Fig.4(b) shows, due to simplifying the algorithm when it been implemented in FPGA.

Fig.4 Sub-channel division

## 5 CDAS2-DDC

For deep space exploration application, it is better to observe the radio source with wide-band mode and spacecraft with narrowband mode. Furthermore, for DOR tune, multi-bit sampling may get higher performance. In this case, the backend need DDC algorithm and will expand the sample bit from 2-bit to 4-bit, 8-bit and 16-bit.

Now the CDAS2-DDC has been installed in several CVN stations. Fig.6 shows the device installed in SH station. A commercial server has taken the place of Mark5 as a recorder.

Fig.6 CDAS2-DDC and recorder

Fig.7 shows the fringes between two CDAS2-DDC devices that installed in SH and T6 station. The observation mode is 2MHz x 16 channels.

Fig.7 fringes between SH and T6

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