Content

- DBBC hardware characteristics
  - What is it good for
  - A tour around the DBBC
  - Component description
- Installation of a DBBC
- DBBC software
  - Poly-phase Filter Bank (PFB)
  - Digital Down Conversion (DDC)
- Basic testing
- Field System integration
- VLBI operation
The VLBI backend

- Antenna Feed LNA
- Backend
- Recorder Network Correlator

IF Band Forming → Base Band Forming → Stream10GE VDIF
The DBBC Architecture

IFn (MHz)
1~512, 512~1024, 1024~1536, 1536~2048
or
1~1024, 1024~2048 MHz
DBBC Outside (front view)
DBBC Outside (rear view)
IF input and the analog conditioning module - CoMo
DBBC Inside

Timing and clock board - CaT2

Stack with FilaIN, ADB1/2, Core2Boards, and FilaOUT
DBBC Inside
The DBBC Architecture

DBBC2 / DCCB2010 Schematic Top View
The DBBC Architecture

The air cooling flow from a side view
General Features

- 4/8 RF/IF Input out of 16 (4x4) in a range up to 2.2 (3.5) GHz
- 1024/2048 MHz sampling clock frequency
- Several personalities for different observing modes
- Input 4/8 polarizations / bands
- Output 4/8 groups of 32 data channel
- Output as VSI interfaces or as 10G Ethernet streams
- Control under Field System or other client console
1. Analog Conditioning Module – CoMo
2. Analog-Digital Converter (ADB1 / ADB2)
3. Data Processing (Core2)
4. Connection and Service (FiLaIN/OUT – FiLa10G FILA10G-4)
5. Timing and Clock (CaT2 – Clock and Timing)
6. Computer Control (PCSet)
1. Conditioning Module (Unica3)

- 4 selectable RF inputs
- 4 selectable Nyquist filters
- 31.5 dB programmable attenuation
- Total power full band
- Manual or automatic gain control
1. Conditioning Module (Unica4)

- Now with: 8 selectable Nyquist filters
- 2 Unica boards build 1 CoMo
2. Analog to digital converter ADB1/2

- Analog input: 0 - 2.2 GHz
- Max Sampling clock 1.5 GHz
- Max Instantaneous bandwidth 750 MHz (real) / 1.5 GHz (complex)
- Output data 2 x 8-bit @1/4 Sclk DDR

- Analog input: 0 – 3.5 GHz
- Max sampling clock 2.2 GHz
- Max instantaneous bandwidth 1.1 GHz (real) / 2.2 GHz (complex)
- Output data 2 x 8-bit @1/4 Sclk DDR
  4 x 8-bit @1/8 Sclk DDR
- Piggy pack module support for 10-bit output and connection to Fila10G
3. Basic processing unit - Core2

- Input rate:
  
  \[
  (4 \text{ IF} \times 2 \text{ bus} \times 8\text{-bit} \times \text{SClk/4 DDR}) \text{ b/s} \\
  (2 \text{ IF} \times 4 \text{ bus} \times 8\text{-bit} \times \text{SClk/8 DDR}) \text{ b/s} 
  \]

- Typical output rate:
  \[
  (64 \text{ ch} \times 32\text{-}64\text{-}128) \text{ Mb/s}
  \]

- Programmable architecture
  - Digital down conversion (DDC)
    1 Core2 = 4 BBCs
  - Poly-phase Filter Bank (PFB)
    1 Core2 = 16 Poly-phase filters

- 1 VSI 32 channel output
First and Last board in the stack

- First: IN
  - Communication interface
  - JTAG programming channel
  - 1pps in

- Last: OUT
  - 2 VSI interfaces
  - 1pps monitor out
  - 80 Hz continues calibration out
Complete Module Stack
6. PC Set – Control computer

Adventech PCI-7030: Half Size PCI Motherboard (Intel Atom) on PCI backplane

ADLink PCI7200: Communication with 32-bit bus for Core2 register setting, total power measurement, state statistics, etc.

ADLink PCI9111HR: Communication with Conditioning Modules for IF total power measure, automatic gain control, registers control, etc.

Xilinx programmer: FPGA device configuration through USB – JTAG interface

Adventech PCI-7030: Half Size PCI Motherboard (Intel Atom) on PCI backplane
Installation of a DBBC

How to connect the DBBC

- 10 MHz
- H-Maser 1PPS
- 1PPS test out
- 80 Hz cont cal
- RF/IF input
- Monitor
- Keyboard
- Mouse
- Network
- VSI-H
Installation of a DBBC

- e-VLBI 10 GE switch
- Mark5B+ disk recorder
- Counter to monitor gps – 1pps out (MK5B)
- DBBC
- Field System PC
Installation of a DBBC

4x4 IF-Splitter to provide all possible IFs at the DBBC
Inputs:
IF1: a. 500-1000 IF RCP
b. 0-500 IF RCP
c. 500-1000 IF LCP
d. 0-500 IF LCP
IF2: a. 500-1000 IF RCP
b. 0-500 IF RCP
c. 500-1000 IF LCP
d. 0-500 IF LCP
IF3: a. 500-1000 IF RCP
b. 0-500 IF RCP
c. 500-1000 IF LCP
d. 0-500 IF LCP
IF4: a. 500-1000 IF RCP
b. 0-500 IF RCP
c. 500-1000 IF LCP
d. 0-500 IF LCP
blank – sync generation from 80 Hz
FiLa10G (SA)

- Two independent 10G Ethernet UDP port
- Physical interface optical XFP
- 10G port fully bidirectional
- Installed inside the DBBC box or as stand-alone
- Data rate: 1 – 2 – 4 Gbps each 10G port
- Format mode: RAW, MK5B or VDIF
FiLa10G Software

• FILA10G Files:
  c:\DBBC\bin\timesyncFILA10G.exe (MK5B time set)
  c:\DBBC\bin\vdif_timesyncFILA10G.exe (VDIF time set)
  c:\DBBC\bin\sendstr.exe (serial communication)
  c:\DBBC_conf\FilesDBBC\fila10g_v3.3.1.bit
  c:\DBBC\doc\DBBC2 FILA10G Command set v3.3.1.pdf

Note: a program to sync with a NTP server is required
(eg. NetTimeSetup-314.exe) or new FiLa10G modules
have a GPS module build in that can be used to get the
GPS time.
Setting up the FiLa10G

• Upload of the firmware is
  - automatically made by the DDC/PFB control software (internal FiLa10G)
  - done with an additional Xilinx JTAG programmer using a script for IMAPCT (external FiLa10G-SA)
• Communication is through serial port or Ethernet in the stand-alone version
• Commands available (see document)
• VDIF packet size setting (see document)
• Script files can be used for block of commands (see batch)
Observing modes

- **DDC**: tunable, channel bandwidth between 1 MHz and 64 MHz, U&L, Continuous cal with 80 Hz synchronization, modes: geo, astro, astro2, w-astro, lba, test
- **PFB**: fixed tuning, channel bandwidth 32/64 MHz, all U or L depending on the Nyquist zone
- **DSC**: full 4 x 512/1024 MHz, max 8 x 1024 MHz band direct sampling conversion, all U or L depending on the Nyquist zone
- **SPECTRA**: 4Kch/IF spectrometer, max 32K channels
Conversion to baseband, tunable channels of variable bandwidth
Conversion to baseband, fixed channels
PFB – poly-phase filter bank

Nyquist zone 1 / 3

USB 1
USB 2
USB 3
USB 4
USB 5
USB 6
USB 7
USB 8
USB 9
USB 10
USB 11
USB 12
USB 13
USB 14
USB 15
USB 16

0 MHz
1024 MHz
512 MHz
1536 MHz

Nyquist zone 2 / 4

LSB 16
LSB 15
LSB 14
LSB 13
LSB 12
LSB 11
LSB 10
LSB 9
LSB 8
LSB 7
LSB 6
LSB 5
LSB 4
LSB 3
LSB 2
LSB 1

1024 MHz
2048 MHz
512 MHz
1536 MHz
How the observing mode is selected

• Using a dedicated firmware
• Using a dedicated control software
• Using a dedicated configuration text file
Files Structure:

C:\DBBC\bin
→ control software

C:\DBBC\doc
→ manuals

C:\DBBC_CONF\n
→ configuration text files

C:\DBBC_CONF\FilesDBBC
→ firmware
There are 5 files, weighing 36.9 MiB with 59 hits in DBBC2-DDC.

Displaying 1 to 5 of 5 files.

**DBBC2-DDC**

- [DBBC2 DDC v105](https://www.hat-lab.cloud/downloads-dbdc2-ddc/) (3.1 MiB - 6 hits - 20 April 2018)
- [DBBC2 DDC v106_261118.rar](https://www.hat-lab.cloud/downloads-dbdc2-ddc/) (9.9 MiB - 5 hits - 26 November 2018)
- [DBBC2 DDC v107_beta1.zip](https://www.hat-lab.cloud/downloads-dbdc2-ddc/) (6.8 MiB - 16 hits - 20 November 2018)
- [DBBC2 DDC v107_beta2.rar](https://www.hat-lab.cloud/downloads-dbdc2-ddc/) (8.4 MiB - 9 hits - 11 January 2019)
- [DBBC2 DDC v107_beta3.rar](https://www.hat-lab.cloud/downloads-dbdc2-ddc/) (8.7 MiB - 23 hits - 30 January 2019)
Software

• DDC:
  c:\DBBC\bin\DBBC2 Control DDC v107.exe (server)
c:\DBBC_conf\dbbc_config_file_107.txt
c:\DBBC_conf\FilesDBBC\dbbc2_ddc_v107.bit
c:\DBBC\doc\DBBC2 DDC command set v107.pdf

• PFB:
  c:\DBBC\bin\DBBC2 Control PFB v16_2.exe (server)
c:\DBBC_conf\dbbc_poly_config_file_16.txt
c:\DBBC_conf\FilesDBBC\dbbc2_pfb_v16.bit
c:\DBBC\doc\DBBC2 PFB command set v16.pdf
Example:

1 dbbc2_ddc_v107.bit 597.00 8 ← the first number is indication of ADB1|2, in this case ADB1 is on
1 dbbc2_ddc_v107.bit 682.00 8 IFA and ADB2 on IFB, ADB1 in IFC, no Core2 for IFD
1 dbbc2_ddc_v107.bit 853.00 8 If no Core2 is inserted in the first and second column put 0.
1 dbbc2_ddc_v107.bit 938.00 8 The second parameter is the firmware file name to be used.
2 dbbc2_ddc_v107.bit 597.00 8 The third and fourth parameters are frequency and bandwidth respectively.
2 dbbc2_ddc_v107.bit 682.00 8
2 dbbc2_ddc_v107.bit 853.00 8
2 dbbc2_ddc_v107.bit 938.00 8
1 dbbc2_ddc_v107.bit 597.00 8
1 dbbc2_ddc_v107.bit 682.00 8
1 dbbc2_ddc_v107.bit 853.00 8
1 dbbc2_ddc_v107.bit 938.00 8
0 dbbc2_ddc_v107.bit 597.00 8 Each Core2 board supports 4 bbcs so if not present 0 has to be inserted in
0 dbbc2_ddc_v107.bit 682.00 8 four lines
0 dbbc2_ddc_v107.bit 853.00 8
0 dbbc2_ddc_v107.bit 938.00 8
1 fia10g_v2_1.bit COM2 ← if installed set 1st version 1 (with ACE), 2nd version (without ACE 2), otherwise 0, ser. port
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values forIFF
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH
107 112 0 0 ← phase calibration values
CAT2 1024 ← CAT1|2 and sampling frequency
PROG 0 3 ← jtag programmer: 0=xilinx, 1=digilent; prog freq. 3/6 MHz
Starting the software

DDC: running **DBBC2 Control DDC v107.exe**

![Image of software interface]

after the Core2 configuration is completed

then run a client ex. **DBBC Client v3.exe** or **Field System**

**DDC Mode Commands** and **Form Table** (see documents)
First tests with the DBBC

- Cabling the DBBC: IF, 1pps, 10 MHz, (80 Hz calibration?)
- Starting the DDC software (server) on the DBBC Windows PC
  - Newest version always available at http://www.hat-lab.cloud currently v105/v106 or v107 beta3 for DDC
- Configuration file needs to be edit for your hardware installation.

First functionality can be tested with the DBBC_client or from the FS:
- select different IF inputs for the ADBs and let AGC adjustment work, e.g.
  > dbbcifa # for query
  > dbbcifa=2,agc,2 # to set RF input 2, agc on, IF filter 2 (0-500 MHz)

read out BBCs set different frequencies, ...
  > dbbc01 # for query
  > dbbc01=596.00,a,16.00 # to set BBC freq=596 MHz, IFA, BBC band width = 16 MHz
First tests with the DBBC

> dbbcifa  # for query
> dbbcifa=2,agc,2  # to set RF input 2, agc on, IF filter 2 (0-500 MHz)

read out BBCs set different frequencies, ...
> dbbc01  # for query
> dbbc01=596.00,a,16.00  # to set BBC freq=596 MHz, IFA, BBC
  band width = 16 MHz
Connecting a Mark5B(+)  

Connect the DBBC VSI1 port to the Mark5B using VSI cable.

Set Mark5B needs to be synced to the 1pps on the VSI cable.
tstDIM > clock_set=32:ext
tstDIM > 1pps_source=vsi
tstDIM > dot_set=:force
tstDIM > dot?  # query several times to see if it stays synced

Test the quality of the connection
DBBC > ddbcform=test,tvg  # starts TVG on the DBBC
tstDIM > tvr=0xffffffff  # TVR LED should be green.

If it is not green it might help to carefully disconnect and reconnect the VSI cable on both ends, sometimes cleaning the connectors with dry air is required.

For testing with a Flexbuff or Mark6 it is recommended to use the FS
Calibration of the DBBC

Calibration or phase optimization is required at the system installation and has to be repeated after a hardware modification in the stack, transportation, or a new firmware. Periodically as a general check.

- Connect a synthesizer tuned to 764 MHz to all Ifs or a broadband IF signal (not too strong).
- Load the firmware to test.
- Point all dbbcifa,b,c,d to this input and set AGC to manual, e.g.
  - `dbbcifa=1,40,1`  # adjusted to about 10000 counts
  - In DDC mode: turn off AGC for BBCs: `dbbcgain=all,20,20`
- Run the DBBC command: `calibration=all`
- ... wait

Description at:
https://deki.mpifr-bonn.mpg.de/GMVA/GMVA_HOWTO/DBBC2_calibration
Calibration of the DBBC
DDC configuration file

c:\DBBC_conf\dbbc_config_file_v107.txt

Example:
1  dbbc2_ddc_v107.bit  597.00  8 ← the first number is indication of ADB1|2, in this case ADB1 is on
1  dbbc2_ddc_v107.bit  682.00  8  IFA and ADB2 on IFB, ADB1 in IFC, no Core2 for IFD
1  dbbc2_ddc_v107.bit  853.00  8  If no Core2 is inserted in the first and second column put 0.
1  dbbc2_ddc_v107.bit  938.00  8  The second parameter is the firmware file name to be used.
2  dbbc2_ddc_v107.bit  597.00  8  The third and fourth parameters are frequency and bandwidth respectively.
2  dbbc2_ddc_v107.bit  682.00  8
2  dbbc2_ddc_v107.bit  853.00  8
2  dbbc2_ddc_v107.bit  938.00  8
1  dbbc2_ddc_v107.bit  597.00  8
1  dbbc2_ddc_v107.bit  682.00  8
1  dbbc2_ddc_v107.bit  853.00  8
1  dbbc2_ddc_v107.bit  938.00  8
0  dbbc2_ddc_v107.bit  597.00  8  Each Core2 board supports 4 bbcs so if not present 0 has to be inserted in
0  dbbc2_ddc_v107.bit  682.00  8  four lines
0  dbbc2_ddc_v107.bit  853.00  8
0  dbbc2_ddc_v107.bit  938.00  8
1  f la10g_v2.1.bit COM2 ← if installed set 1st version 1 (with ACE), 2nd version (without ACE 2), otherwise 0, ser. port
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFA
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFB
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFC
1 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFD
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFE
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values forIFF
0 38000 ← no unica=0 unica3=1, unica4=2, initial CoMos target values for IFH
100 100 100 100 ← phase calibration values
CAT2 1024 ← CAT1|2 and sampling frequency
PROG 0 3 ← jtag programmer: 0=xilinx, 1=digilent; prog freq. 3/6 MHz
Test recordings

- Test recordings are good to control the correct sampling (bit statistics), band pass shape, and pcal tones.

- The Mark5B comes with a set of programs that allow to check the bit statistics (bstate), do auto- or cross correlations (vlbi2), and extract phase cal (bpcal).

- More powerfull are the mark5access programs: m5bstate, m5pcal, m5spec, m5timeseries, ...

  Available from the EVN TOG wiki pages

  https://deki.mpifr-bonn.mpg.de/Working_Groups/EVN_TOG/DBBC/DBBC_Test_Procedures

- jive5ab allows to stream data directly on a local disk, which avoids to record on diskpacks and use disk2file for small tests.
Test recordings

oper@eff-mark5c-1:~$ m5spec

m5spec ver. 1.3.1  Walter Brisken, Chris Phillips  20120508

A Mark5 spectrometer. Can use VLBA, Mark3/4, and Mark5B formats using the mark5access library.

Usage : m5spec <infile> <dataformat> <nchan> <nint> <outfile> [offset]

(infile) is the name of the input file
<dataformat> should be of the form: <FORMAT>-<Mbps>-<nchan>-<nbit>, e.g.:
  VLBA1_2-256-8-2
  MKIV1_4-128-2-1
  Mark5B-512-16-2
  VDIF_1000-64-1-2 (here 1000 is payload size in bytes)

<nchan> is the number of channels to make per IF
<nint> is the number of FFT frames to spectrometize
<outfile> is the name of the output file
<offset> is number of bytes into file to start decoding

The following options are supported
-dbbc    Assume dBBC polarisation order (all Rcp then all Lcp)
-nopol   Do not compute cross pol terms
-help     This list
> bstate

Usage: bstate <input m5b fname> <# frames>

> bstate n13c1_ef_no0002.m5a 200

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Test recordings

- `vlbi2 file1 file2 -proctime proctime [-rev <0|1>] [-2bit <0|1>] [-tforce <0|1>]`
  - 2bit: 1 to enable 2-bit input
  - rev: 1 to reverse channels in the plot
  - tforce: 1 to force correlation, ignoring timestamps
- `vlbi2 n13c1_ef_no0002.m5a n13c1_ef_no0002.m5a -2bit 1`  # for autocorrelation

- `gv dd1.pos`
Test recordings

- `bpcal`
  
  Usage: `bpcal <input m5b frame> <tone freq (KHz)> <# frames>`
  
  Example: `bpcal n13c1_ef_no0002.m5a 2490 500`

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Estimate the best IF level

• IF commands (dbbcifa, or ifa (FS)) allow to specify values for the IF target counts where the AGC should adjusted to.

• With an increasing number of DBBCs the best target IF levels seem to cluster around 35000 to 45000 counts, but it might be worth to test those for your DBBC.

• Best to use with a true receiver with phase-cal on.

• Then change the attenuation in steps of 2.5 dB over the whole range, while checking detector counts, bbc counts and doing some short 10 sec recordings at the Mark5B

• Analyse the recordings using bpcal to measure the Pcal-tone amplitudes.
Estimate the best IF level

Figure 2: Phase-cal amplitude calculated by bpcal over 0.15 sec against detector counts.
The DBBC2 is fully integrated into the Field System:

- It supports both PFB and DDC firmware.
- Continues calibration in DDC mode.
- With and without Fila10G.
- Allows synchronization to internal GPS or NTP on FS-PC.

### EFLSBERG equipment:

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Press <ret> or type 0 for no change. Else <rack><rec1><rec2><start>

CAUTION! Be sure the schedule works with your choices!
Field System integration

• Notes on DBBC2 integration are available in /usr2/fs/misc/dbbc.txt

• There are the typical control-files that need to be adapted for a new backend and one special for the DBBC IP address:
  • `dbbad.ctl` hold the DBBC IP address
  • `equip.ctl` for the FS
  • `skedf.ctl` for DRUDG
  • Some more in `point.prc`, `station.prc`, and `.Xresources`

→ Once this is done the FS should be ready to DRUDG and observe DBBC schedules.
define proc_library 00000000000x
" EUR135   EFLSBERG Ef
" drudg version 2015Jan29 compiled under FS  9.11.07
"< DBBC    rack >< Mark5B   recorder 1>
enddef
define exper_initi 00000000000x
proc_library
sched_initi
logsw_jv
mk5=DTS_id?
mk5=OS_rev?
mk5=SS_rev?
mk5=status?
enddef
define setspxx    00000000000x
pcalon
tpicd=stop
mk5b_mode=ext,0x55555555,,8.000
mk5b_mode
form=geo
form
dbbcsx4
ifdsx
cont_cal=on,4
bbc_gain=all,agc,12000
tpicd=no,200
bank_check
tpicd
enddef

define dbbcsx4 00000000000x
bbc01=100.99,a,4.00
bbc02=110.99,a,4.00
bbc03=140.99,a,4.00
bbc04=200.99,a,4.00
bbc05=310.99,b,4.00
bbc06=390.99,b,4.00
bbc07=440.99,b,4.00
bbc08=460.99,b,4.00
bbc09=112.99,c,4.00
bbc10=127.99,c,4.00
bbc11=137.99,c,4.00
bbc12=167.99,c,4.00
bbc13=187.99,d,4.00
bbc14=192.99,d,4.00
enddef
define ifdsx 00000000000x
ifa=4,agc,2,38000
ifb=4,agc,2,38000
ifc=2,agc,2,38000
ifd=2,agc,2,38000
lo=loa,8110.00,usb,rcp,1
lo=lob,8110.00,usb,rcp,1
lo=loc,2100.00,usb,rcp,1
lo=lod,2100.00,usb,rcp,1
enddef
Field System integration
Field System integration
Field System integration

Field System Log

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System Status

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|          | SCHED-none LOG-station PRES | 984.7mb DEC | 33d09m (2000) | | | |
|          | ISTC | ITS | ITS | ITS | ITS | | |
|          | 0 | 0 | 0 | 0 | 0 | |

NO CHECK: rx

ERRORS

System Temperature

Operator Input
DBBC2 resources

- DBBC2 software, firmware and documents:
  http://www.hat-lab.com (until 2018)
  https://www.hat-lab.cloud

- DBBC2 installation, testing, and operational notes:
  https://deki.mpifr-bonn.mpg.de/Working_Groups/EVN_TOG
  https://deki.mpifr-bonn.mpg.de/GMVA