Mark 5 Memo #5

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TO: Distribution

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SUBJECT: Preliminary design specifications for Mark 5 VLBI data system

Introduction

The Mark 5 system is being developed as the first high-data-rate VLBI data system based on magnetic-disc technology. With sustained data rates of 1024 Mbps and capacity limited only by the ever-increasing capacity of magnetic discs, the Mark 5 represents a radical departure from the traditional VLBI dependence on magnetic tape.

Background

In September 1999, a Haystack Observatory white paper [Ref 1] stated the goals of a next-generation Gbps VLBI data system and concluded that the computer industry was rapidly developing the basic technology which could lay the groundwork for inexpensive implementation.

In May 2000 Haystack Observatory proposed to pursue the development of a new high-data-rate VLBI data system based mostly on commercial-off-the-shelf (COTS) technology. Phase I of this proposal, funded by NASA, USNO, NRAO and EVN/JIVE, sought to identify the appropriate recording technology, to be followed by a Phase II development program.

The focus of Phase I was initially on commercial magnetic-tape systems, which had seen rapid improvements over the past few years. Prime candidates were multi-drive DLT and LTO systems. At the time, LTO was a newcomer but showed much promise in fulfilling a role in VLBI data systems. An LTO drive was actually obtained from Hewlett-Packard for testing, and preliminary tests were promising [Ref 2].

All of this changed in early January 2001 when a study of price data for tape and disc clearly showed an accelerating price decline for discs vs. tape, in concert with disc-industry projections for dramatic continued disc improvement in terms of cost per unit storage [Ref 3]. It was clear that, in terms of storage costs, discs were highly likely to overtake tape within a very few years. Additionally, off-the-shelf COTS technology relating to the desktop PC was rapidly advancing to provide a inexpensive support infrastructure around which to develop a disc-based Gbps VLBI data system. From that point on, all attention for a new VLBI data has focused on discs, particularly the inexpensive garden-variety discs with IDE/ATA interfaces.

Mark 5 Demonstration System

A market survey was made of possible COTS components that might be assembled into a demonstration disc-based VLBI system. Various avenues were pursued, including various vendors of RAID equipment and interfaces. At that time, no vendor of RAID equipment could really come close to offering a solution to sustained read and write at 1 Gbps supported by a single host PC. Multiple-host systems were considered, but appeared to be awkward to implement a full-fledged VSI-H-compliant system. The chosen solution was a combination of a specialized disc interface from Boulder Instruments (model StreamStor 816) and a high-speed I/O card (model HPDI32) from General Standards Corporation. The combination of these two cards allowed us to construct and demonstrate a system in early March 2001 which could record actual VLBI data at 576 Mbps from a Mark 4 formatter spread over an array of 16 IDE disc drives, but could play it back at only 288 Mbps. In addition, the demonstration system was connected to the Mark 4 correlator at Haystack Observatory and actual VLBI fringes were obtained [Ref 3].

Mark 5 Design Goals

Though the Mark 5 demonstration system showed the feasibility of a disc-based VLBI data system, it certainly did not meet the full set of design requirements for an operational Gbps Mark 5 system. The goals established for an operational Mark 5 system are:

- Minimum of 1024 Mbps data rate
- Design based primarily on unmodified off-the-shelf subsystems and components
- Modular, easily upgradeable as better/cheaper technology becomes available
- Robust operation, low maintenance cost
- Short initial design cycle and delivery of operational units to the field
- Compatibility and interoperability with existing Mark 4 and VLBA data and correlator systems, with evolution to conformance with the VLBI Standard Interface (VSI) specification
- Flexibility to support electronic transfer ('e-VLBI') and computer processing of recorded data
- Easy transportability
- Minimum 24-hour unattended operation at 1 Gbps

Mark 5 Design Decisions

Following the success of the simple Mark 5 demonstration system, a full re-evaluation was undertaken to determine its strengths and weaknesses in order to lay the ground work for the development of an operational Mark 5 system. The following shortcomings were noted:

1. The StreamStor 816 card worked well, but the necessity to move the data over the available 32-bit/33-MHz PCI backplane proved to be a major bottleneck, particularly during playback[1].
2. The 800 Mbps limit of the StreamStor was below the target of 1024 Mbps.

[1] During recording, the demonstration system moved data over the PCI bus directly from the I/O card to the StreamStor card. During playback, due to limitations of the I/O card, the data had first to be read from the discs into main memory, then transferred out through the I/O card, effectively doubling the usage of the PCI bus.

3. The 1-MB buffer available on the General Standard digital I/O card was insufficient.
4. The data-rate capability of the General Standards I/O card was insufficient (640 Mbps max).

Haystack Observatory entered into discussions with Boulder Instruments regarding possible modifications to overcome these shortcomings. In particular, the following was proposed:

1. Provide an external I/O interface directly on the StreamStor card. This removes the data from the PCI bus, as well as removing the expensive ($4K) commercial digital I/O card. The I/O interface is specified to conform to the industry-standard FPDP specification [Ref 4] and will reside on a card-top bussable connector.
2. Improve the data-rate capability of the StreamStor card to sustain minimum 1056 Mbps (32 bits @ 33 MHz), which gives a bit of headroom above 1024 Mbps.
3. Incorporate a large buffer on the StreamStor card to buffer between the external I/O port and the disc array.

Haystack has subsequently entered into an agreement with Boulder Instrument to augment the StreamStor card with these upgrades, and also including the following:

1. Support for 64-bit/66-MHz PCI bus standard, which is becoming increasingly available, and which can easily move data at ~2 Gbps aggregate rate.
2. Support for a triangle of Gbps data connectivity between 1) the external I/O port, 2) the disc array and 3) the PCI bus, though only connection between any two is supported at a single time. In each connection case, the large on-board buffer will be active.
3. During recording, dynamic load shifting among discs in array to compensate for slow or failed disc.
4. On playback, a user-specified data-fill pattern will be supplied during data breaks which might otherwise be caused by slow or missing discs; data continuity and synchronization through such events is thus guaranteed.

With these changes to the StreamStor card, the basic block diagram of the Mark 5 system becomes as shown in the Figure 1. Two custom boards are required to build the Mark 5 system, an 'Input Board' to buffer data between the VLBI data source and the FPDP bus, and an 'Output Board' to buffer data between the FPDP bus and the VLBI data sink.

FPDP Bus

The Front Panel Data Port (FPDP) is an industry-standard bus [Ref 4] intended to provide high-speed data transfer between two or more boards. Originally developed for the VME-bus community, its use has now broadened to other communities as well, including a number of commercial PC-based interface cards

Figure 2 shows the FPDP bus structure to be used on the Mark 5, which is implemented as a flat-ribbon cable spanning top-edge FPDP connectors on the Input Board, the Output Board and the StreamStor interface cards. It consists of 32 data lines (D<31:0>, a clock line (+/-PSTROBE), plus three status and handshake lines (NRDY*, DVALID*, SUSPEND); the details and usage of these signals is specified by the FPDP standard [Ref 4]. The interface cards can be configured to use the FPDP bus in two modes:

Record/Bypass Mode: In this mode, the Input Board is the data source, which is received simultaneously by the StreamStor and Output Boards. The StreamStor may record this data at the user's option.

Playback Mode: In this mode, the StreamStor card provides data to the Output Board for presentation to the user. The Input Board is idle.

The usage of the FPDP is standard *except* during Playback mode, where the Data Clock is supplied by data sink instead of the data source. This is done so that the output data rate can be easily controlled by the Output Card, which is highly desirable for flexibility of usage at the correlator.

Note that during Record/Bypass mode the Output Board receives the data stream from the Input Board. This allows full testing of the Input and Output Boards independently of the StreamStor card. In addition, this capability allows multiple Mark 5 systems to be cascaded ('daisy-chained') together to any depth, each receiving and regenerating the data stream to the next, as illustrated in Figure 3. This type of cascaded connection of Mark 5 systems is useful, for example, in expanding the total data capacity at a station for longer periods of unattended operation, as data recording is sequenced from one system to another.

Disc-Data Format

A 32-bit word is transferred to the StreamStor card on each PSTROBE clock cycle of the FPDP bus; successive words are accumulated into a 64 kB logical buffer. This 64 kB buffer is then written to one disc in the disc array. Successive 64 kB buffers of data are directed to the disc array in round-robin fashion; that is, each disc in turn receives a 64 kB buffer, moving cyclically through the discs in the array. Note that this format automatically spreads the data from all channels over all discs. Consequently, the loss of data from a single disc during playback will be spread the data loss equally over all channels.

Two-Stage Mark 5 System Development

In order to deliver useful Mark 5 systems to the field as quickly as possible, a two-stage development program is being undertaken:

Mark 5A: The Mark 5A system is designed to be a direct hardware replacement for a Mark 4 or VLBA tape transport at either a field station or at a correlator. At a field station, it requires use with a Mark 4 or VLBA formatter. Maximum aggregate data rates are 1024 Mbps for Mark 4 and 512 Mbps for VLBA systems (equivalent of 64 tape tracks in each case).

Mark 5B: The Mark 5B system will be fully VSI compatible [Refs 5,6] with 1024 Mbps maximum aggregate date rate, though it will also maintain some backwards compatibility with Mark 4 and VLBA systems (see Supported Record/Playback Modes)

The Mark 5A System

The Mark 5A system is designed to be a *direct plug-compatible replacement for a Mark 4 or a VLBA tape recorder at either a field station or a correlator,* except that:

1. The Mark 5A can record and playback only exactly 32 or 64 'tracks' of data from a Mark 4 or VLBA formatter[2].
2. The software control of the Mark 5A is somewhat different, but is vastly simplified from a Mark 4/VLBA tape transport.

The Mark 4 formatter can output up to 64 tracks of data at 18 Mbps/track, which includes the parity overhead, for a total of 1152 Mbps. However, it is not necessary to record the parity bits in the low-error-rate environment of the discs; therefore, the Mark 5A Input and Output interface cards do some special processing to remove the parity bits for recording and restore them on playback. In particular:

Mark 5A Input Board (block diagram in Figure 4):

3. All parity bits are removed.
4. In 32-track mode (equivalent to Mark 4/VLBA headstack 1 only), the resulting 32 parallel bit streams are sent directly to the FPDP bus for recording.
5. In 64-track mode (equivalent to Mark 4/VLBA headstack 1 and 2), adjacent even and odd track-pairs are interleaved bit-by-bit before being sent to the FPDP bus. Maximum data rate at this point will be 1024 Mbps for Mark 4 and 512 Mbps for VLBA[3].

Mark 5A Output Board (block diagram in Figure 5):

32-track mode: The Output Board synchronizes to the data stream by searching one of the 32 FPDP bit streams for a Mark 4/VLBA 'sync word' followed by the appropriate CRC sequence[4]; the 'tracks' are assumed to be synchronized with each other. Parity is restored and the data are sent to the user as 32 normal Mark 4 or VLBA tracks.

64-track mode: The Output Board synchronizes to the data stream by searching one of the 32 FPDP bit-streams for two interleaved 'sync words' followed by two appropriate interleaved CRC sequences. The 32 track-pairs are de-multiplexed, parity is restored, and the data are sent to the user as 64 normal Mark 4 or VLBA tracks.

The Output Board will automatically recognize whether data is in 32 or 64-track mode and act accordingly.

Data Clocking

The Input Board is driven by data and clock from the Mark 4 or VLBA formatter at a maximum frequency of 18 MHz. In turn, the Input Board drives the FPDP bus with data and clock at an average frequency 8/9 (32-track case) or 16/9 (64-track case) times the formatter clock frequency.

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[2] Only 32 or 64 'tracks' can be recorded; no other number of tracks is allowed. Both Mark 4 and VLBA formatters can be configured to multiplex a single channel to 1, 2 or 4 tracks with 1-bit samples or to 2, 4 or 8 tracks with 2-bit samples, so that 32 or 64 tracks can normally be filled with data.

[3] Actual maximum data rate for VLBA is slightly higher (516.096 Mbps to be exact) due to non-data-replacement nature of the format.

[4] Sync word without parity consists of 4 contiguous bytes of 1's. The CRC character is not contiguous, but follows a specific number of bits later (different for Mark 4 and VLBA).

The Output Board has two clock modes:

1. In Record/Bypass mode, the Output Board receives data and clock from the Input Board; in turn, the Output Board must synthesize a clock at 9/8 (32-track case) times that rate to present data to the user.
2. In Playback mode, the Output Board generates a clock at the desired user output data rate (via on-board synthesizer or crystal with 2^n divider network, or optional external user input). This clock frequency is multiplied, on average, by 8/9 (32-track case) or 16/9 (64-track case) to create the FPDP clock.

Mark 5A Software Control

The control of the Mark 5A system is quite simple and requires a minimal command set:

Record/Bypass commands:
- Setup
  - Set 32 or 64-track Record/Bypass mode on Input Board
- Action
  - Start recording (automatically appends to existing recording)
  - Stop recording
  - Erase recording (reset record pointer to zero)

Playback commands:
- Setup
  - Set playback rate (if clocked by crystal or synthesizer on Output Board)
- Action
  - Set playback start position (byte number)
  - Start playback
  - Stop playback (system will automatically revert to Bypass mode)
  - Skip forward/backward specified # of bytes (while playing back); for synchronization

Status/information commands:
- Report current position (byte number of recorded data)
- Report disc serial numbers
- Report general system status

The details of the command syntax and content will be negotiated with the intended users of the systems during the development period. Control will be via an RS-232 serial port (like Mark 4/VLBA) and also possibly Ethernet, implemented on a Linux OS.

The Mark 5B System

The Mark 5B system will be fully VSI-H and VSI-S compatible [Refs 5, 6]. A VSI-compatible Mark 5B Input Board and Mark 5B Output Board will be designed to replace the Mark 5A Input and Output Boards for full VSI-compatible operation.

Mark 5B Data Format on Disc

The proposed Mark 5B data format on disc is based on the standard non-data-replacement VLBA-format tape frame [Ref 7], but *with all parity bits removed*, which we call a Data Frame. The serial bit stream on each on the 32 FPDP data lines is composed of Data Frames, analogous

to Mark 4/VLBA 'tracks' and, as we shall see, largely compatible with playback through a Mark 5A Output Board.

According to VSI-H specification, the allowed number of active input data-streams is 1, 2, 4, 8, 16 or 32. When 32 bit-streams are active, the data from each bit stream are formed into a stream of Data Frames which are transferred to the corresponding FPDP bit-stream. When fewer than 32 input bit-streams are active, the Data Frames from each input bit-stream are spread over a number of FPDP bit-streams corresponding to a '*fan-out factor*', which is defined as 32 divided by number of active input bit-streams, and where each FPDP bit-stream rate is reduced by the fan-out factor. In this way, all 32 FPDP bit-streams are always fully utilized.

Each Data Frame contains 20,160 bits (2520 bytes) and consists of five parts, in order (see Figure 6):

1. A 4-byte 'sync word' consisting of all 1's.
2. A 6-byte time-tag corresponding to the VSI 'DOT clock' reading at the instant of the first data bit in the Data Frame; format is MJD format used by VLBA.
3. A 2-byte CRC code which protects the time-tag data field.
4. 2500 data bytes, decimated by the fan-out factor[5].
5. A 4-byte 'user data' field, details not yet specified.
6. A 4-byte-bit 'system data' field containing Mark 5B system and housekeeping information, organized as 8 4-bit BCD characters. If we reference these 8 hex characters as **RRSSBBF0**, in order from left to right, they are grouped into 5 logical subfields:
    a. RR: Reserved
    b. SS: Originating bit-stream number (values 0 to 31 inclusive)
    c. BB: Bit number [values 0 to (fan-out factor–1)]
    d. F: Bit 3 - Data Frame contains invalid data
       Bits 6-0 - Fan-out factor binary exponent (0 to 5); see paragraph below
    e. 0: All zeroes

This format is fully compatible with VLBA correlators at a record rate up to 512 Mbps (32 tracks @ 16 Mbps/track). However, if the Mark 5B extends the same format to 1024 Mbps across 32 tracks, the recording appears as 32 'tracks' @ 32 Mbps/track, which is incompatible with Mark 4/VLBA correlators[6].

Special Mark 5A 64-track Compatibility Mode

In order to overcome the 512 Mbps limitation, the Mark 5B will incorporate a special 'Mark 5A compatibility mode' which records data to disc in the same format as the Mark 5A 64-track mode. Thus, *data recorded with a Mark 5B Input Board may be played back through a Mark 5A Output Board in either 32 or 64-track mode*.

[5] This is exactly analogous to the way Mark 4 and VLBA do data fan-out.

[6] It might be possible to modify the correlators to accept data recorded in this fashion. However, the current limitations of 16 Mbps/track for Mark 4 correlators and 8 Mbps for the VLBA correlator would force a drastic slowdown in data processing time compared to recording time.

Supported Record/Playback Modes

Since both Mark 5B and the 32-track Mark 5A mode both create standard VLBA-compatible Data Frames on each of the FPDP bit-streams, there is much inherent interoperability between Mark 5A and Mark 5B systems. Table 1 summarizes the various supported combinations of Mark 5A and Mark 5B.

Input Board	Input Board mode	Max aggregate record rate (Mbps)	Output Board	Max aggregate playback rate (Mbps)	Comments
5A	32-trk	512 (Mark 4) 256 (VLBA)	5A	1024	Input data from Mark 4/VLBA formatter; 32 trks in/out; max useful playback rate is 512 Mbps to Mark 4 correlator and 256 Mbps to VLBA correlator. Direct connection to 32-trk Mark 4/VLBA correlator in place of tape transport..
5A	64-trk	1024 (Mark 4) 512 (VLBA)	5A	1024	Input data from Mark 4/VLBA formatter; 64 trks in/out; max useful playback rate is 1024 Mbps to Mark 4 correlator and 512 Mbps to VLBA correlator. Direct connection to 64-trk Mark 4/VLBA correlator in place of tape transport.
5A	32-trk	512 (Mark 4) 256 (VLBA)	5B	1024	32 trks in from Mark 4/VLBA formatter; VSI out. Mark 5B Output Board must ignore 'system data' part of aux data and be instructed externally; implies 5B OB must recognize Mark 4 format Data Frames
5B	Normal	1024	5B	1024	VSI in/out
5B	Normal	512	5A	1024	VSI in; 32-trk Mark 4/VLBA out; Max fan-out ratio is 4 for Mk4/VLBA compatibility. Reproduces 32 VLBA-compatible tracks. Direct connection to 32-trk Mark 4/VLBA correlator in place of tape transport.
5B	Special Mk5A 64-trk compatibility mode	1024	5A	1024	VSI in; 64-trk Mark 4/VLBA out. Max fan-out ratio is 4 for Mk4/VLBA compatibility; Direct connection to 64-trk Mark 4/VLBA correlator in place of tape transport.

Table 1: Supported record/playback modes

As you will note, with the addition of the special Mark 5B Input Board '64-track compatibility mode' described above, interoperability between Mark 5A and Mark 5B is essentially complete. The implications of this statement is important, because it implies that *data recorded on either Mark 5A or Mark 5B systems may be processed on either Mark 4/VLBA-compatible or VSI-compliant correlators*[7].

[7] The only caveats are that 1) the fan-out ratio on recording must not exceed four and 2) data recorded with a Mark 5B Input Board (VSI interface) and targeted at a 64-track Mark 4 or VLBA correlator must be recorded in the special '64-trk compatibility mode'. If targeted at a VSI correlator, 64-track data must be recorded in 'normal' mode since the Mark 5B Output Board will not understand data written in the special 64-track compatibility mode. Note further, however, that such 64-track data recorded in 'normal' mode could still be processed at a Mark 4/VLBA correlator by playing it back through a 5B Input Board/5A Output Board combination, as explained in the following section.

Upgrade to VSI Interface on Mark 4/VLBA Correlators

Careful observers will already have noted that it is possible to implement a full VSI-compatible interface on an existing Mark 4 or VLBA correlator by simply placing the combination of a Mark 5B Input Board and Mark 5A Output Board in front of the normal input to the correlator, as shown in Figure 7. A StreamStor card is not needed. The Input/Output board combination is simply placed in Bypass mode so that incoming VSI data is directly transformed into VLBA-compatible tracks.

Of course, if a StreamStor card is added to this combination in the normal way, as shown in Figure 8, a single Mark 5 system can provide the dual function of a normal Mark 5 reproduce system as well as a VSI interface for connection of an external VSI-compliant playback system!

Triangle of Connectivity

The StreamStor card implements a 'triangle of connectivity' schematically illustrated in Figure 9. The three vertices are the disc array, the FPDP bus and the 64-bit/66-MHz PCI bus, buffered by a common 256 MB memory. The StreamStor card can move data at 1-Gbps between any two of these vertices, but only one path can be active at one time. The following options therefore exist:

1. FPDP to/from disc array: This is the path used for normal recording of data directly from a VLBI data-acquisition system or directly to a correlator system. In this case, the data do not touch the PCI bus.
2. PCI to/from disc array: This path may be used to read disc data onto the PCI bus for either local processing or transmission of pre-recorded disc data over an e-VLBI network connection to a correlator. Alternatively, e-VLBI data received over a network connection may be moved from the PCI bus to the disc array for local buffer storage at the correlator.
3. PCI to/from FPDP: This path may be used at a station for direct real-time e-VLBI data transmission to a correlator or, in reverse, at a correlator to receive e-VLBI data and send it directly for processing.

This flexibility of connectivity allows the Mark 5 to fit naturally into the world of e-VLBI, both with real-time and buffered data transmissions. With today's technology it is likely that two standard Gigabit-Ethernet connections operating simultaneously will be required to transmit or receive a full 1-Gbps, but 10-Gigabit Ethernet is expected soon which will easily handle 1 Gbps on a single network connection.

Possible Future Enhancements

There has been much comment about the relatively high price and uncertain long-term availability of the StreamStor card. In the short term, we feel the StreamStor approach is the most suitable for quickly developing and deploying a 1-Gbps disc-based VLBI data system which can naturally evolve to a fully VSI-compatible system. It is clear, however, that cheaper, more commodity-like components will continue to appear which challenge the StreamStor approach. For example, commodity RAID controllers supporting IDE discs are becoming quite competent and inexpensive. And even the capability built into inexpensive motherboard is impressive and improving; Ari Mujunen of Metsahovi Radio Observatory has done some very interesting investigation in this area [Ref 8].

One recent example of such technology is the Escalade series of controllers from 3Ware; for example, the Escalade 7800, one of the first based on 64-bit PCI technology, claims a sustained write rate of 180 MBps and read rate of 127 MBps, which is close to meeting the requirements of sustained 1-Gbps (actually 1024 Mbps = 128 MBps); the price for one such controller is ~$600.

When this type of technology becomes capable of sustained read and write rates of 128 MBps on a reliable real-time basis, it *will be possible to replace the StreamStor card* with an interface card which simply buffers the data between the FPDP bus and the PCI bus. The StreamStor card already has this capability in its FPDP-to-PCI bus mode, so the StreamStor card can be used to test controllers such as the Escalade in a fully operational VLBI mode. The design of such a buffer card is relatively straightforward and would be a natural evolution of the Mark 5 system.

References

1. "Concept for an Affordable High-Data-Rate VLBI Recording and Playback System", 30 Sep 1999, MIT Haystack Observatory, Mark 5 memo 1.
2. "Interim report on COTS-VLBI Phase I study" by Alan R. Whitney, 24 Jan 2001, Mark 5 memo 2.
3. "Second interim report on COTS-VLBI project" by Alan R. Whitney, 8 Mar 2001, Mark 5 memo 3.
4. FPDP Specification, available at http://www.fpdp.com/.
5. "VLBI Standard Hardware Interface Specification –VSI-H", Revision 1.0, 7 August 2000, available at http://gemini1.haystack.edu/vsi/index.html
6. "VLBI Standard Software Interface Specification – VSI-S", under development.
7. "Mark IIIA/IV/VLBA Tape Formats, Recording Modes and Compatibility - Rev 1.2" by Alan R. Whitney, 28 Sep 2000, Mark 4 memo 230, available at ftp://gemini1.haystack.edu/pub/mark4/memos/index.html
8. "The Sustained Disc Streaming Performance of COTS Linux PC's" by Ari Mujunen, Metsahovi Radio Observatory, 13 Jul 2001, available at http://kurp.hut.fi/vlbi/instr/pcwr.pdf and as Mark 5 memo 4.

Note: Mark 5 Memo Series is available at ftp://gemini1.haystack.edu/pub/mark5/index.html

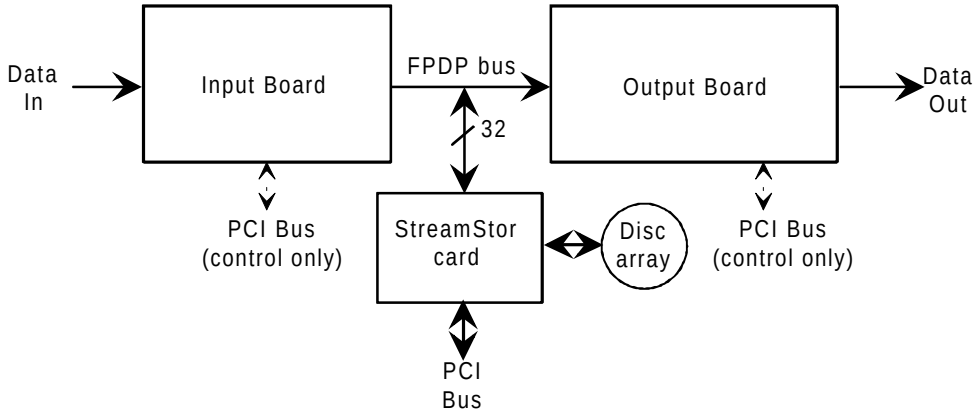

Figure 1: Mark 5 Basic Block Diagram

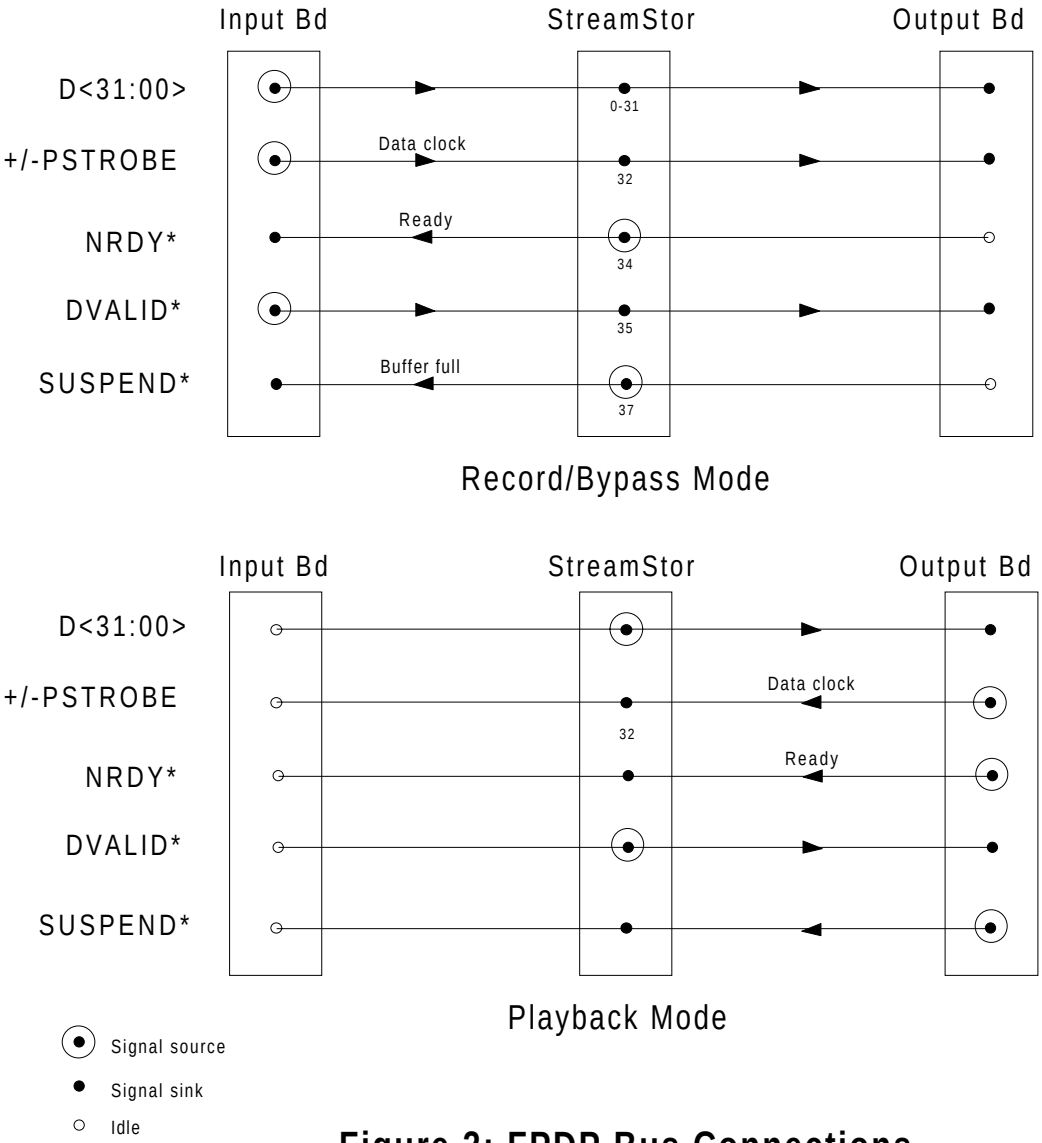

Figure 2: FPDP Bus Connections

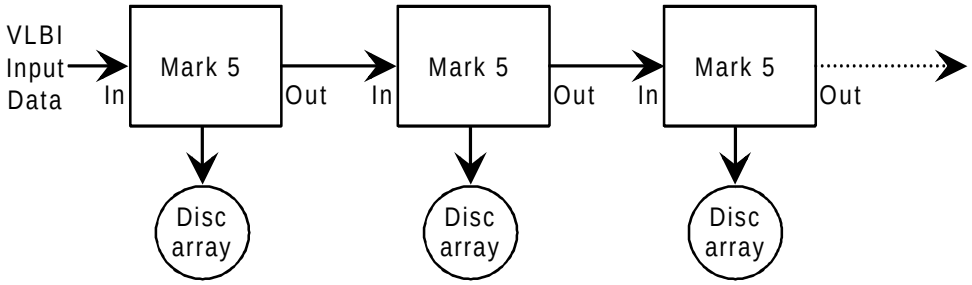

Figure 3: Data-Recording with Cascaded Mark 5 systems

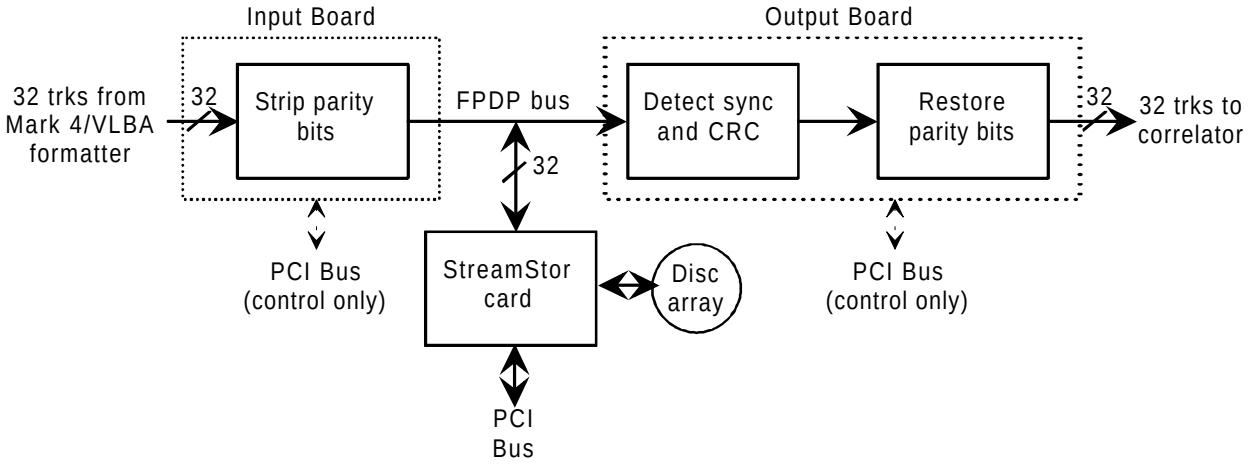

Figure 4: Mark 5A 32-track mode

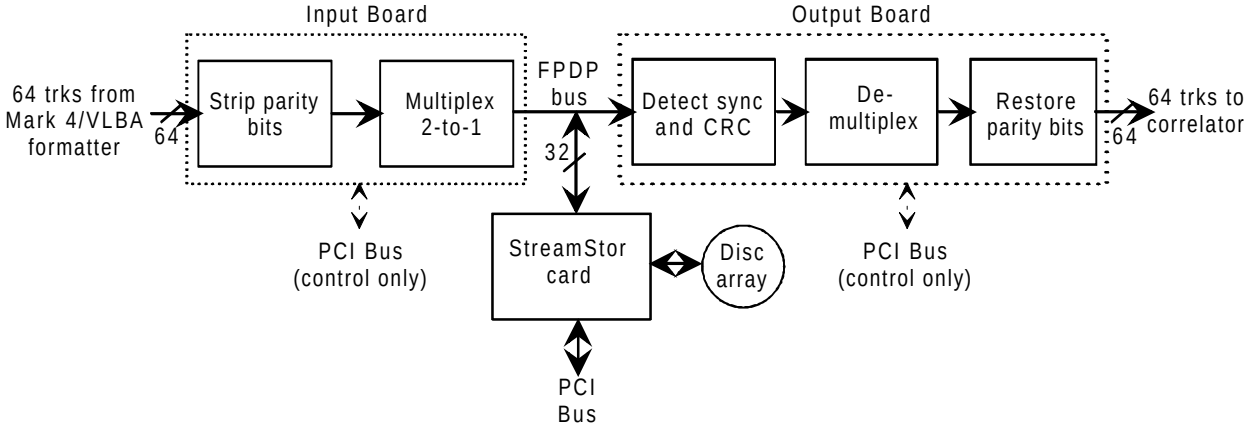

Figure 5: Mark 5A 64-track mode

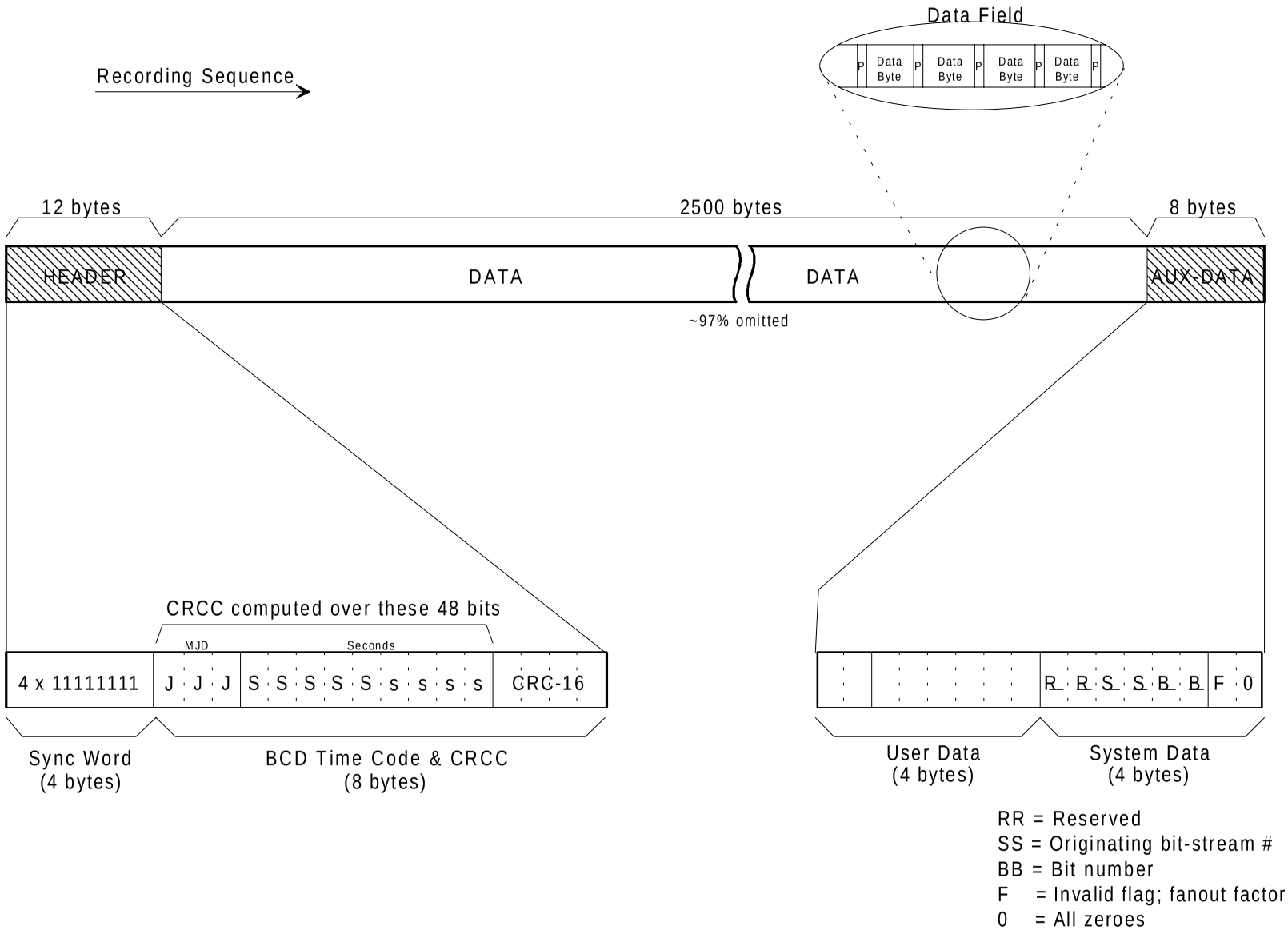

Figure 6: Mark 5B Data Frame Format

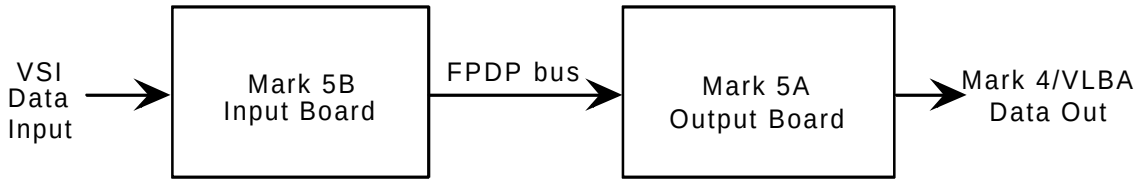

Figure 7: VSI Interface on Mark 4/VLBA Correlator

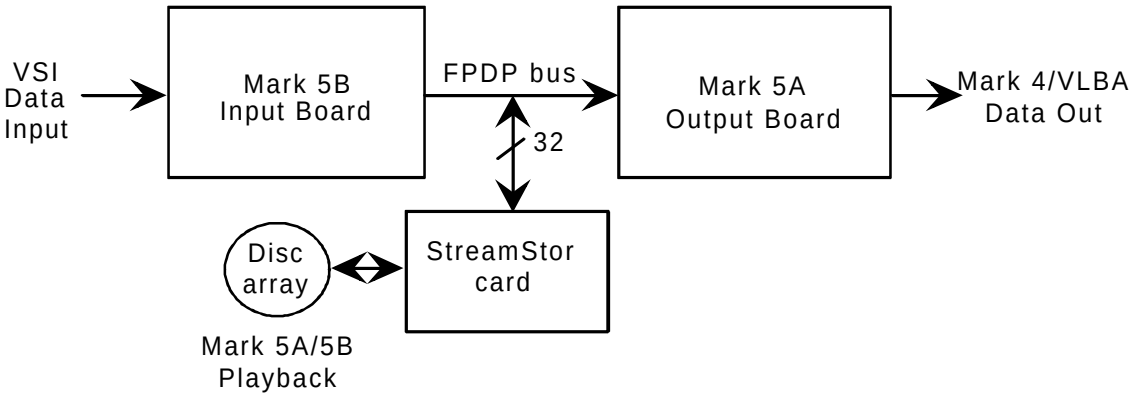

Figure 8: Dual-Function Interface on Mark 4/VLBA Correlato

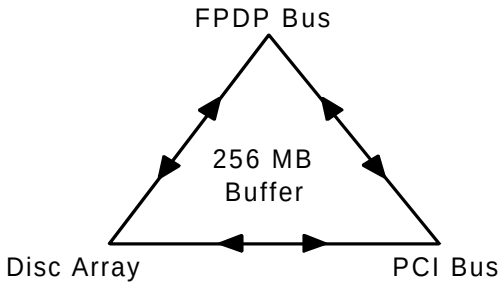

Figure 9: StreamStor 'Triangle of Connectivity'