MARK 5 MEMO #013

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To: Mark 5 Development Group

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Subject: Mark 5A Operating Modes

Introduction

The Mark 5A data recording and playback system operates in ten distinct modes as described below. All modes can operate with VLBA data format or with Mark IV data format. In every case, the FPDP bus, which is the transmission medium from input board to StreamStore board to output board, has 32 active data channels.

Bypass Modes

Bypass mode is so named because the data may flow from the input board to the output board without necessarily being recorded by the disk system. It is characterized by the fact that the time base for the transmission of the data streams is provided by the input board.

Straight Through

In this mode, data is not modified as it passes from input board to output board. No sync detection is performed. The input data rate, the FPDP data rate, and the output board data rate are the same. DVALID* is always asserted and the FPDP clock (PSTROBE/PSTROBE*) runs constantly. This mode is equivalent to the Mark 5P bypass mode.

VLBI Fan out x4 (See Figure 1)

In this, and all other VLBI modes, parity bits are stripped from the data streams by the input board. The parity bits are re-calculated by the output board and re-inserted into the data streams as they are sent out.

Each VLBI data stream (track) is fanned out to four data lines on the FPDP bus in the manner directed by Mark 5 Memo #011.1.
The FPDP clock is transmitted at the track clock rate, with the data being actually passed across the FPDP bus when the DVALID* signal is asserted. Because of the data fan out and the suppression of parity, the DVALID* will be asserted for one FPDP clock edge and then will be de-asserted for a number of clock edges. The edges skipped will alternate between 3 and 4 so that 8/9 of the original data streams will be passed over the FPDP bus.
In this mode there are eight independent VLBI tracks sent over the FPDP bus.

VLBI Fan out x2 (See Figure 2)

Parity bits are stripped from the data streams by the input board. Parity bits are re-calculated by the output board and re-inserted into the data streams as they are sent out.
Each VLBI data stream (track) is fanned out to two data lines on the FPDP bus in the manner directed by Mark 5 Memo #011.1.
The FPDP clock is transmitted at the track clock rate, with the data being actually passed across the FPDP bus when the DVALID* signal is asserted. Because of the data fan out and the suppression of parity, the DVALID* will be asserted for one FPDP clock edge and then will be de-asserted for a number of clock edges. In this case, the edges skipped will be in the sequence 1,1,1,1,2, …
In this mode there are 16 independent VLBI tracks sent over the FPDP bus.

VLBI Fan out x1 (See Figure 3)

Parity bits are stripped from the data streams by the input board. Parity bits are re-calculated by the output board and re-inserted into the data streams as they are sent out.
Each VLBI data stream (track) is altered only by the fact that the parity bits do not appear on the FPDP bus.
The FPDP clock is transmitted at the unaltered track clock rate, with the data being actually passed across the FPDP bus when the DVALID* signal is asserted. Because there is no fan out, the DVALID* signal is only de-asserted when the parity bits appear on the bus. Eight successive bits will be sent, and the ninth (parity) will be "skipped".
In this mode there are 32 independent VLBI tracks sent over the FPDP bus.

VLBI Fan in x2 (See Figure 4)

Parity bits are stripped from the data streams by the input board. Parity bits are re-calculated by the output board and re-inserted into the data streams as they are sent out.
In this mode, 64 VLBI data streams are fanned in to be transmitted on the 32 data lines of the FPDP bus in the manner directed by Mark 5 Memo #011.1.
The FPDP clock rate is higher than that of the track clock. The FPDP clock consists of a "doublet" pulse which is produced in response to each track clock. Each rising edge of the doublet pulse causes 32 bits to be transferred on the FPDP bus. Eight doublets will carry data, followed by a doublet which will be ignored as caused by the de-assertion of DVALID*.

In this mode there are 64 independent VLBI tracks sent over the FPDP bus.

Playback Modes

Playback mode is characterized by the fact that the data are retrieved from the disk system. The time base for the transmission is produced by the output board. The input board is not active on the FPDP bus during playback.

Straight Through

In this mode the 32 tracks which are retrieved are not modified by the output board. No sync detection is performed. The FPDP clock runs continuously. This mode is equivalent to the Mark 5P playback mode.

VLBI Fan out x4 (See Figure 5)

In this and all other VLBI playback modes, the parity bits which are not recorded on the disks are re-calculated and are re-inserted in the playback streams by the output board. Each VLBI data stream is re-constructed from its four FPDP data streams in a reversal of the process used by the input board when the data were recorded. Eight VLBI output streams are re-constructed in this mode.
The FPDP clock runs to extract the data from the disk system until it is time to insert parity into the re-constructed VLBI data streams. At this point the FPDP clock pauses for one extra clock period to allow the parity bits to join the data streams. No data is extracted from the disk system while the FPDP clock is paused.

VLBI Fan out x2 (See Figure 6)

Each VLBI data stream is re-constructed from its two FPDP data streams in a reversal of the process used by the input board when the data were recorded. Sixteen VLBI output streams are re-constructed in this mode.
The FPDP clock runs to extract the data from the disk system until it is time to insert parity into the re-constructed VLBI data streams. At this point the FPDP clock pauses for one extra clock period to allow the parity bits to join the data streams. No data is extracted from the disk system while the FPDP clock is paused.

VLBI Fan out x1 (See Figure 7)

Each VLBI data stream is transmitted as it was recorded. Thirty two VLBI data streams are output in this mode.
The FPDP clock runs continuously to extract the data from the disk system until it is time to insert parity into the re-constructed VLBI data streams. At this point the FPDP clock pauses for one clock period to allow the parity bits to join the data streams. No data is extracted from the disk system while the FPDP clock is paused.

VLBI Fan in x2 (See Figure 8)

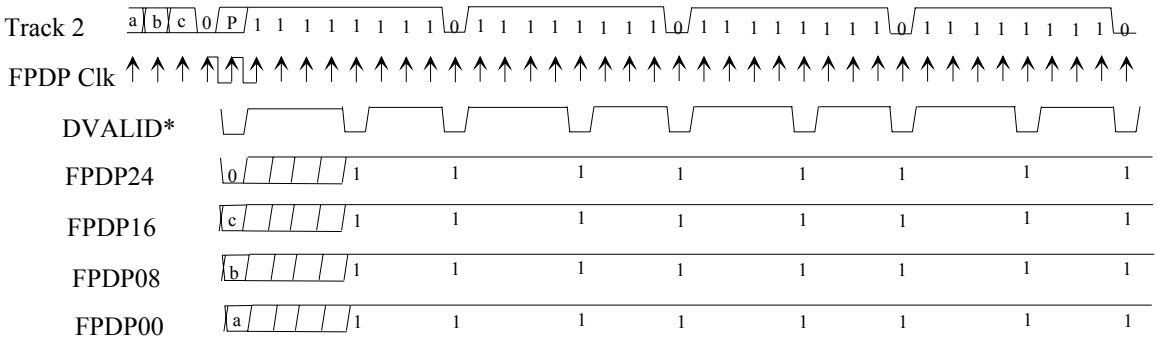
Sixty four VLBI data streams are re-constructed from disk data in this mode.

The FPDP clock runs continuously to extract the data from the disk system until it is time to insert parity into the re-constructed VLBI data streams. At this point the FPDP clock pauses for two clock periods to allow the parity bits to join the data streams. No data is extracted from the disk system while the FPDP clock is paused.

Bypass Mode

Fanout x4

Track 2 to FPDP at Sync



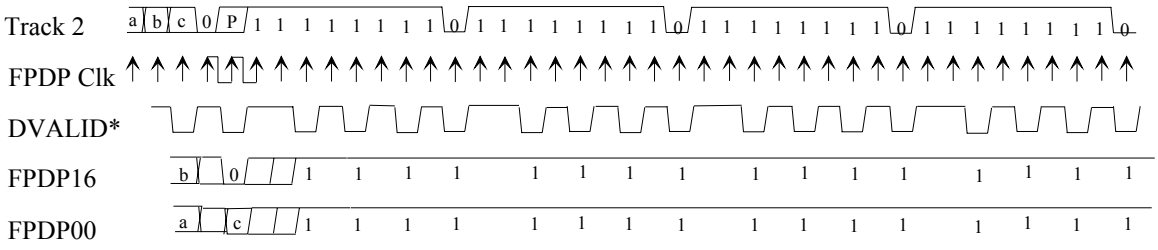
NOTE: There may be a pipeline delay of the signals on the FPDP bus with respect to the VLBI data. A delay of one track clock period is shown.

Figure 1

Bypass Mode

Fanout x2

Track 2 to FPDP at Sync



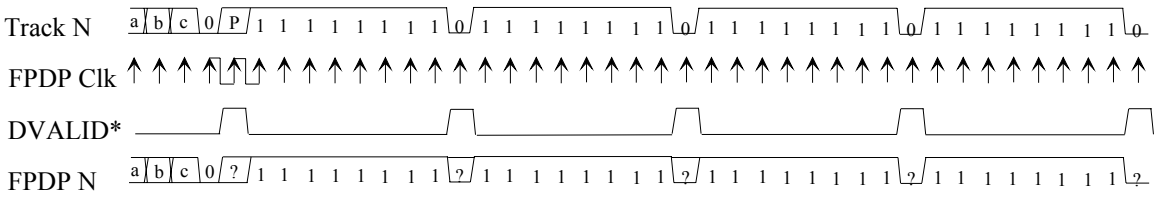
NOTE: There may be a pipeline delay of the signals on the FPDP bus with respect to the VLBI data. A delay of one track clock period is shown.

Figure 2

Bypass Mode

Fanout x1

Track N to FPDP N at Sync



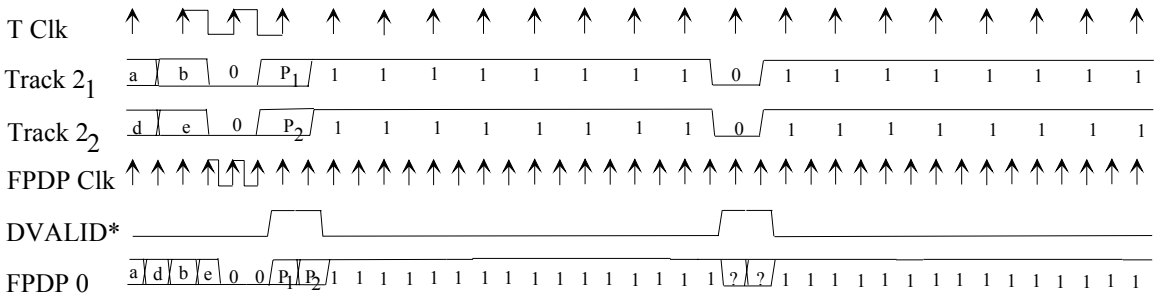
NOTE: There may be a pipeline delay of the signals on the FPDP bus with respect to the VLBI data. A delay of zero is shown.

Figure 3

Bypass Mode

Fan in x2

Track 2, Heads 1 and 2, to FPDP 0

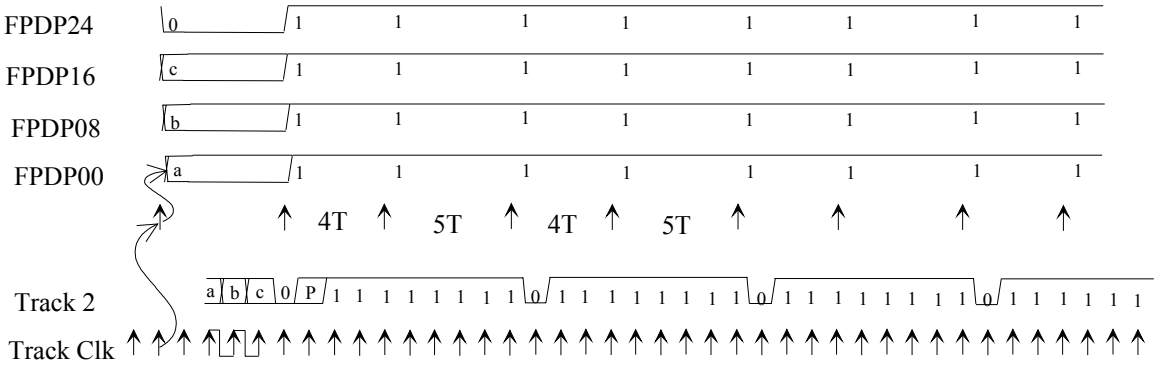


NOTE: There may be a pipeline delay of the signals on the FPDP bus with respect to the VLBI data. A delay of zero is shown.

Figure 4

Playback Mode

Fanout x4



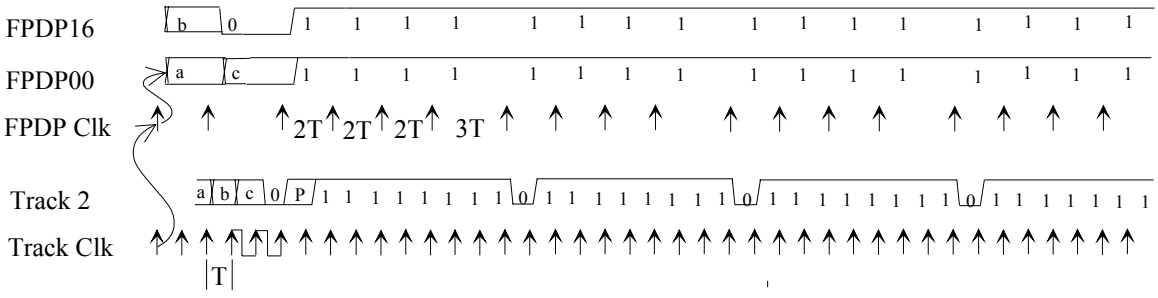
NOTES: FPDP Clock is derived from Track Clock, which is generated by Output Board.

Pipeline delay from FPDP0 to Track 2 is shown as two periods of Track Clock.

Figure 5

Playback Mode

Fanout x2



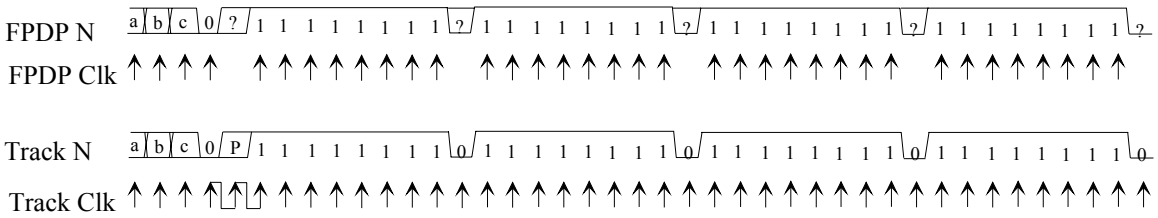
NOTES: Pipeline delay of T from FPDP00 to Track 2.

FPDP clock is derived from Track clock which is generated by output board.

Figure 6

Playback Mode

Fanout x1

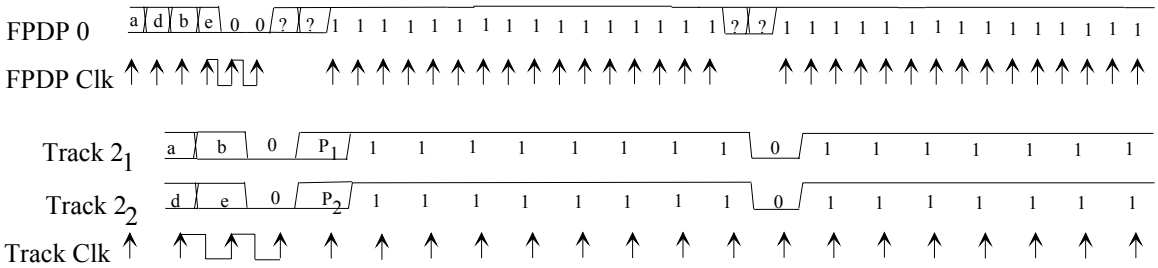


NOTE: There may be a pipeline delay of the signals on Track N with respect to the FPDP bus. A delay of zero is shown.

Figure 7

Playback Mode

Fan in x2



NOTE: FPDP rate is set on output board. Track clock and FPDP clock are derived from a programmable oscillator on the output board.

Figure 8