MARK 5 MEMO #025

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To: List

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Subject: Mark 5B Prototype Test Plan

This document presents a preliminary test plan for the test of the Mark 5B prototype boards. There are currently three boards under assembly, so the test plan can allow a maximum of three Mark 5B boards to be active simultaneously.

Hardware Setups

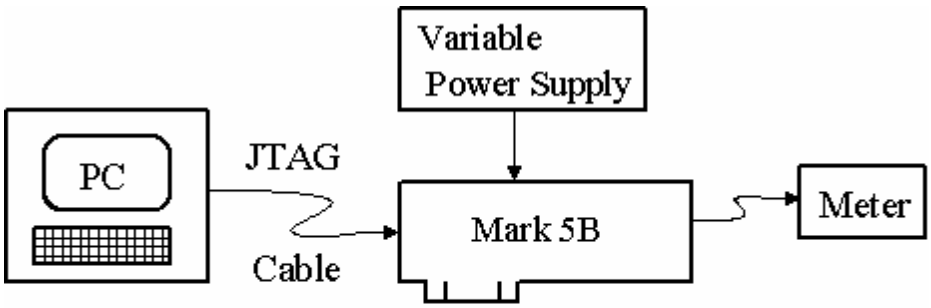

Figure 1
First Test Setup

Figure 1 shows a block diagram of the first test setup. In this setup, the Mark 5B board is not plugged into a PCI connector, but is rather energized with a nominal 5 Volt laboratory supply. This test is not a definitive test of the power distribution system, but serves as a sanity check on the power distribution system. The 5 Volt supply will be set at 5.50 Volts and at 4.5 Volts. The other DC voltages will be probed and should be well within their limits as the FPGA is not configured or operating at this point. Each of the three boards will be given this test for power supply presence.

Boards that have good power distribution will then have their FPGA configured with the DIM functionality by way of the Xilinx download cable. (This is not the normal way that the board will be configured in operation, but will verify that the configuration code is correct and can be loaded for electrical debug.)

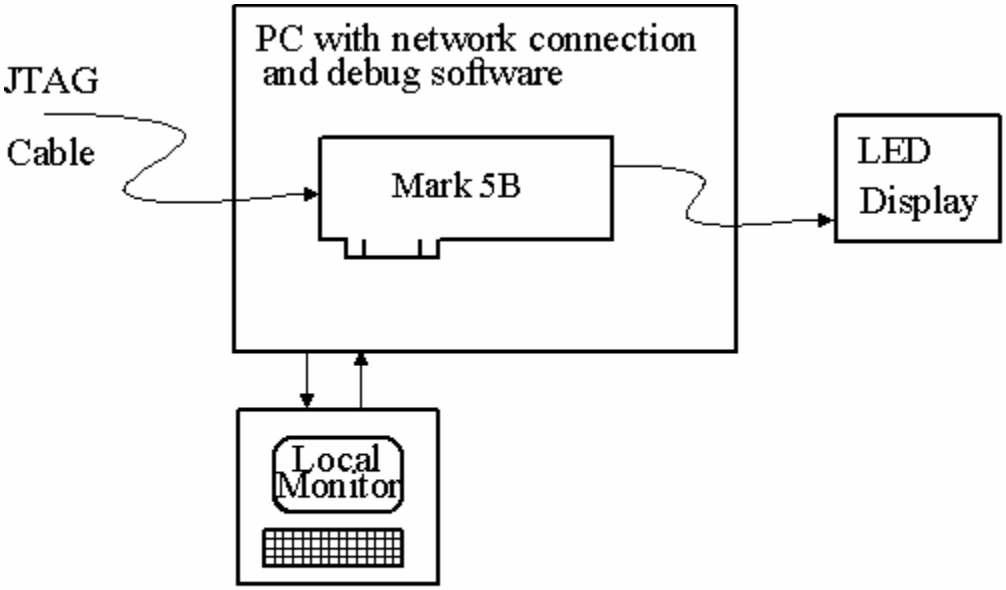

Figure 2

Second Test Setup

In figure 2, the second test setup is shown. In this case the Mark5B board is plugged into a PC and is accessed from the motherboard via the PCI connection. Configuration with DIM functionality is still supplied via the Xilinx download cable as was done in setup number one.

Verification of the ability of test software to access and set the parameters of the DIM will be done. Setup of the local clock generator can be verified. Operation of the software controlled LED's can be verified.

A primary goal of this setup is the development of test support software and the development of the software ability to drive the configuration of the FPGA. For software configuration, jumpers are changed on the board so that the configuration sequence comes from the GPIO pins of the PLX chip. Software on the motherboard reads a configuration file and drives the GPIO pins in a JTAG sequence to cause the configuration to appear in the EEPROM's. Software can then cause the configuration to enter the FPGA and can verify that the configuration is correct.

It is anticipated that this setup will be operational for the time required to do the software development. It is not necessary that the software configuration process be developed in order to proceed to setup number 3.

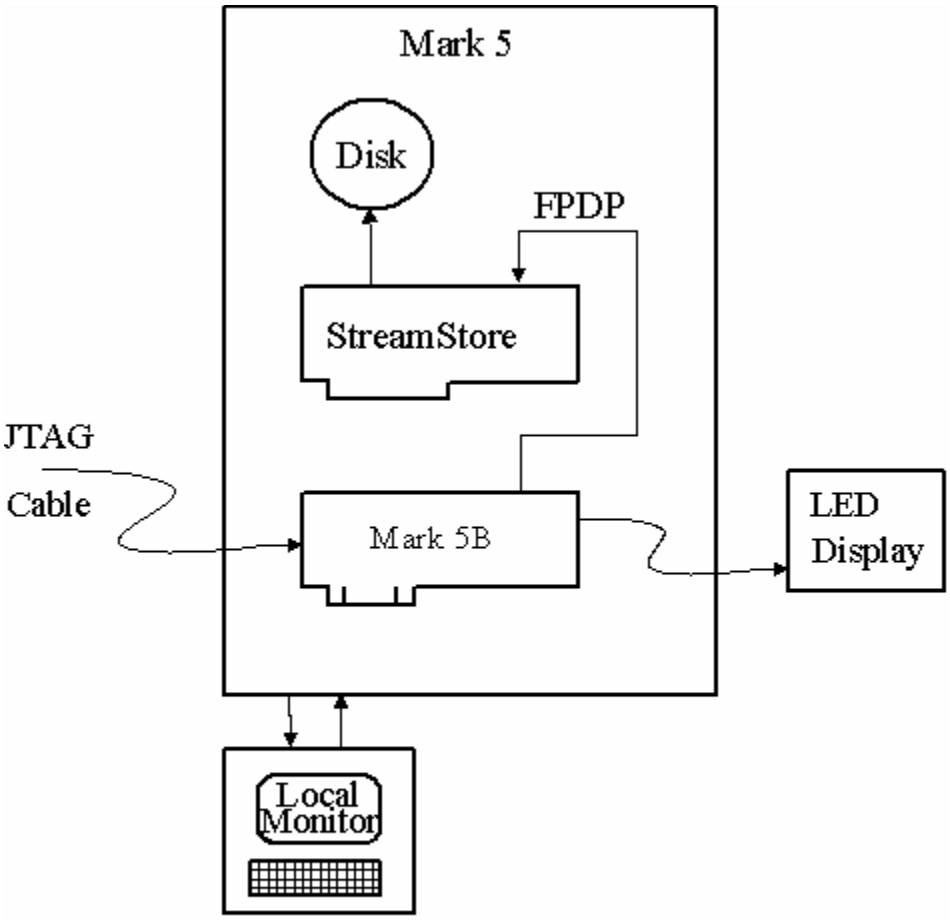

Figure 3

Third Test Setup

In the third test setup, we require a Mark 5 chassis with StreamStore card and disk. The primary goal in this setup is the use of the DIM configuration to write Mark 5B files. The data will be produced by the test vector generator and will consist of VSI test pattern or a pattern of constantly increasing counts (also generated by the TVG). The disk is to be checked by the software's ability to read the disk directly.

This setup allows the test of the DIM's ability to generate Mark 5B files with correctly formatted headers and to put such files on the disk by way of the FPDP bus.

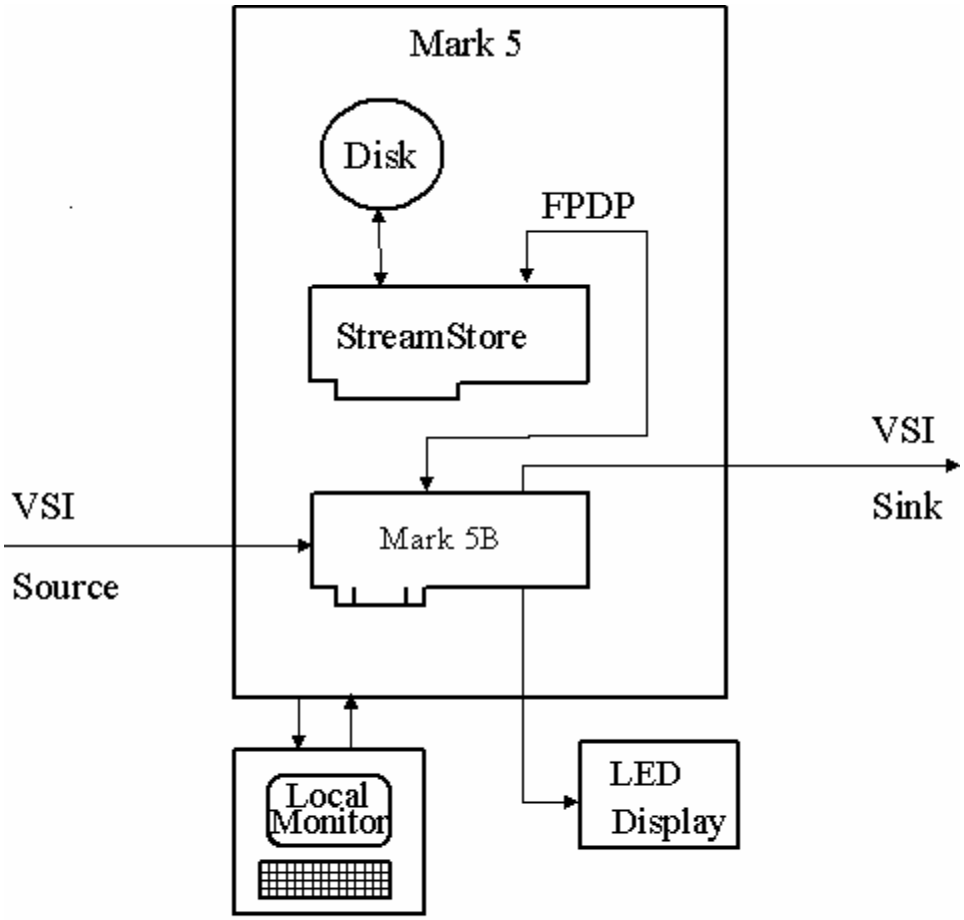

Figure 4

Fourth Test Setup

The fourth test setup is a generic diagram for a number of tests. It does not explicitly show the method of FPGA configuration and does not depend on the capability of software configuration. The download cable can be used if the software configuration is not yet available.

The addition of a VSI data source will enable the completion of the DIM testing. This will also give the ability to create disks with real VSI data to augment the testing of the DOM configuration.

The addition of a VSI data sink is required to assist the debug of the DOM functionality. The DOM configuration will be loaded, the data will be extracted from the disk via the FPDP bus, and the data will be sent to the VSI data sink.

The operational sink would be the correlator, but this probably will not be used in the early going for reasons of convenience and tolerance of low level errors. (The correlator can produce beautiful results with an error rate of one in ten to the fifth, whereas the Mark 5B board should deliver an error rate of zero.)

A useful VSI data sink in the early testing will be provided by a Mark 5 system with a Mark 5B I/O board configured as a DIM, the assumption being that the DIM functionality is operational by this time in the test cycle.

It has been suggested that it might be convenient if the DOM output data streams were modified to contain the signals VALID, BOCF, and R1PPS instead of some of the normal bit streams. The down side of this "debug mode" is that it requires additional parameter support to turn it on and off or that it is a debug configuration only available during test.

Support Software

Wish list of support software capabilities to support Mark 5B prototype debug:

1) Ability to Read/Write any location in DIM/DOM parameter space. (Is this HACK?)

2) Ability to write a set of parameters with fewer keystrokes than HACK requires. (Specify all the parameters for a particular mode of operation with a single command.) Possibly store several sets for on demand use. ("Load set 1"…"Load set 2"…)

3) Verify that a scan is a correct instance of a Mark 5B scan. Also identify violations of Mark 5B file structure such as wrong size, wrong format, crc error, …

4) Compare two Mark 5B scans for equality.

5) Verify that a sequence of frames is a Mark 5B scan. (Scan number increments, time advances correctly, …)

5) Examine files and find TVG (Test Vector Generator) sequences. Note that in Mark 5B TVG sequences have headers imbedded in them.

Test Tableau

Figure 5 shows the sequence of debug events, which are proposed, and identifies the major participants. Note that when the DIM debug in setup #3 is done, that unit becomes the VSI recorder and joins with setup #4 to assist in the DOM debug.

The availability of VSI data sources and sinks are not shown explicitly in figure 5 (yet) and the time dimensioning has yet to be done with the contribution of all involved.

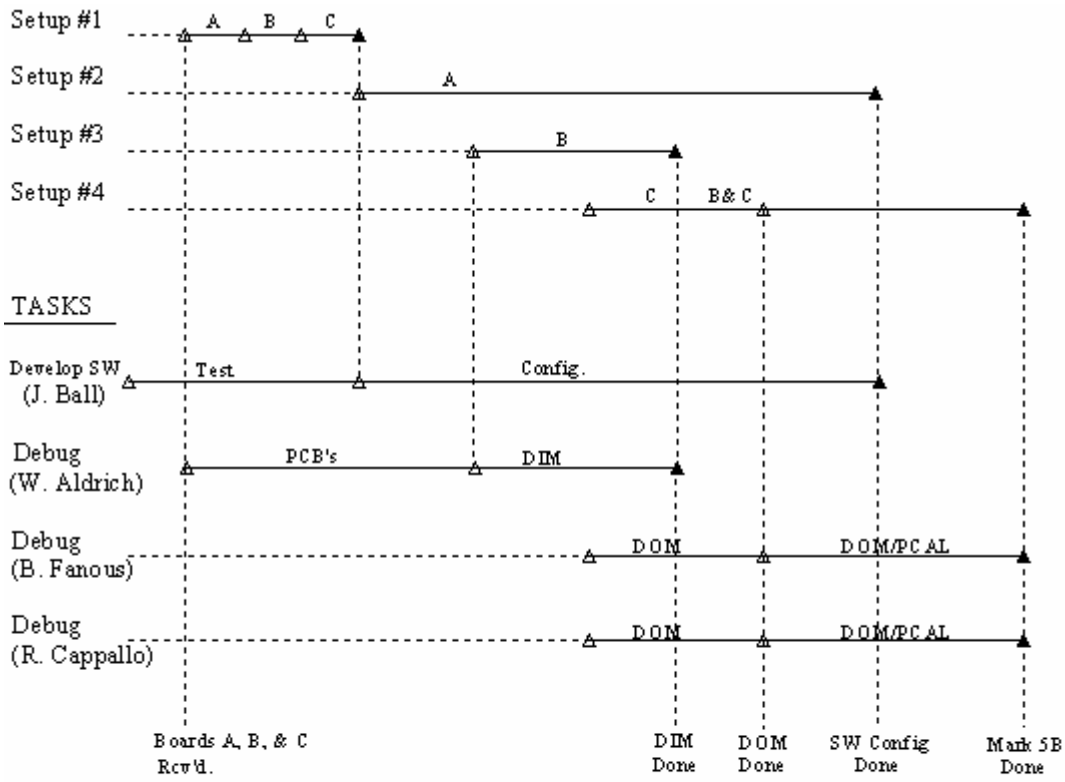

Figure 5

Test Tableau

(Do Not Scale this Drawing)