



ADVANCES IN WIDE-BAND VLBI TECHNOLOGY

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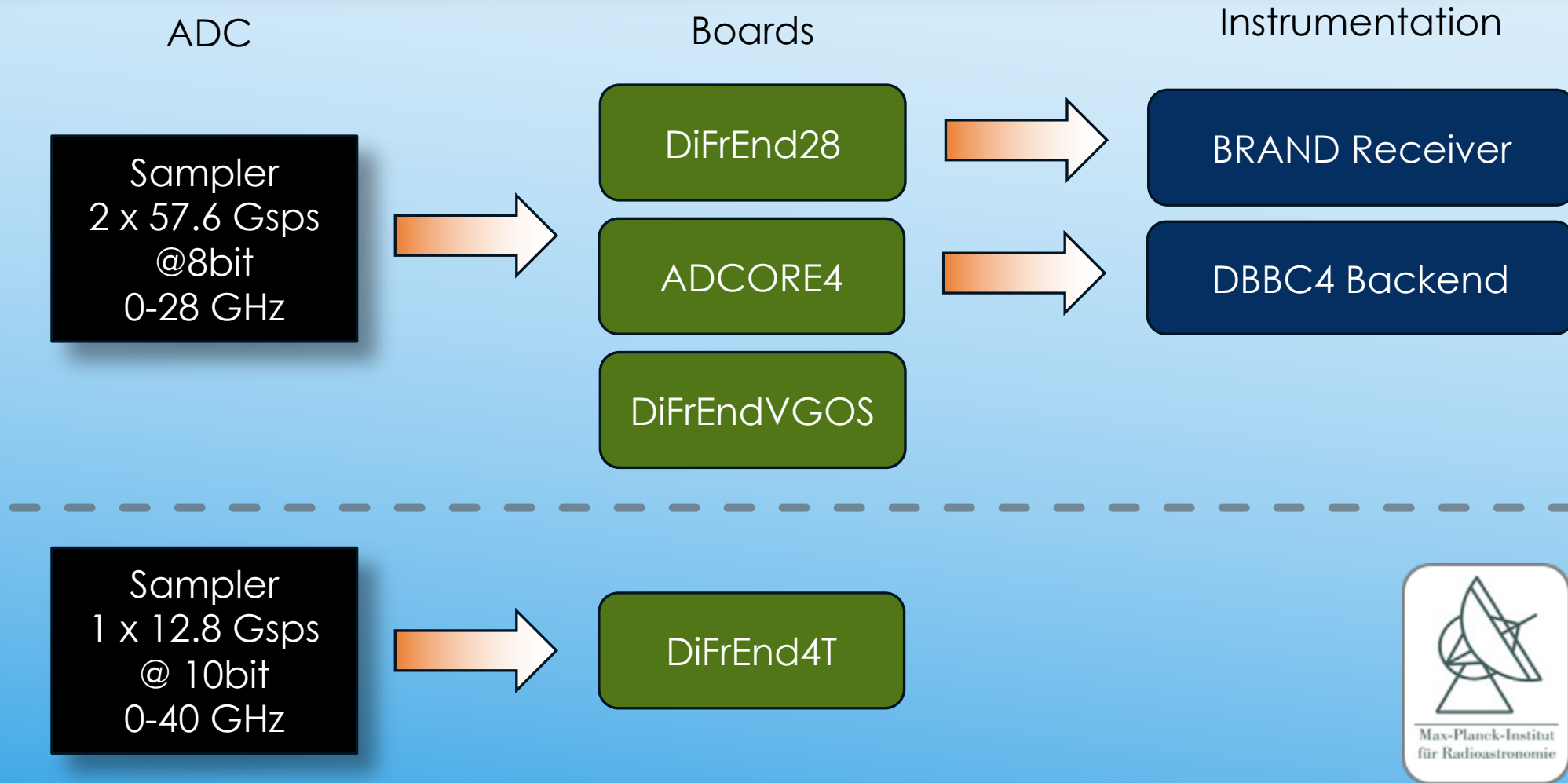
WIDE BAND SCIENCE PERSPECTIVES



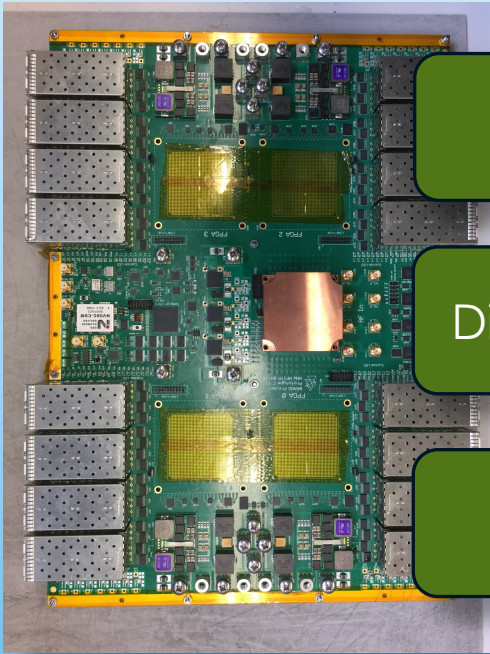
- Improved sensitivity
- Multi-frequency data (more efficient use of observing time)
- Richer spectral information (e.g. line ratios)
- Magnetic field studies (e.g. Faraday rotation)
- Improved calibration (ionosphere, troposphere)
- Phase-stability between bands (astrometry)

Next-generation sampler chips open up opportunities for large increases in the wide-band (VLBI) instrumentation

RECENT DEVELOPMENTS MPIFR / INAF



DIGITAL FRONTEND UNITS



DiFrEnd28

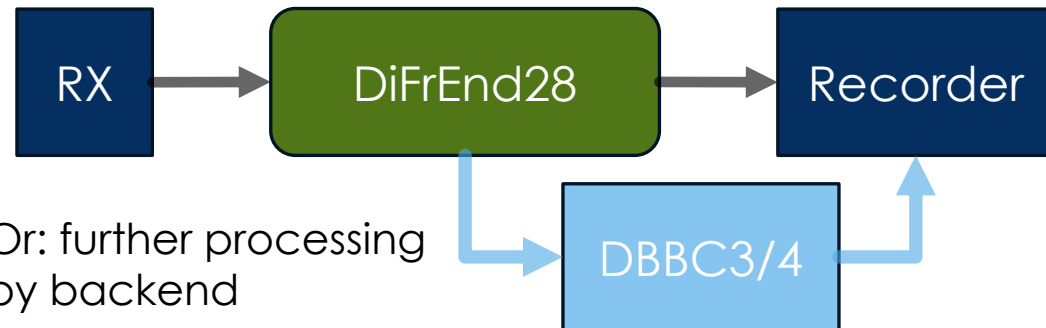
DiFrEndVGOS

DiFrEnd4T

Provide frontend **and** (partial) backend functionality:

- Digitization
- Band filtering (e.g. 512, 1024 MHz etc.)
- Decimation
- VDIF formatting

Minimal VLBI data acquisition system



DIFREND28 – WIDE BAND DIGITAL FRONTEND



Status: under final testing

Sampler chip

- 2 x 57.6 Gsps @ 8 bit
- ENOB: 6.5

PCB

- Dimension: 30 x 40 cm
- Layout: 22 Layers

Digital processing

- 4 FPGA Xilinx Kintex UltraScale
- 1 Tbps data transport to FPGAs

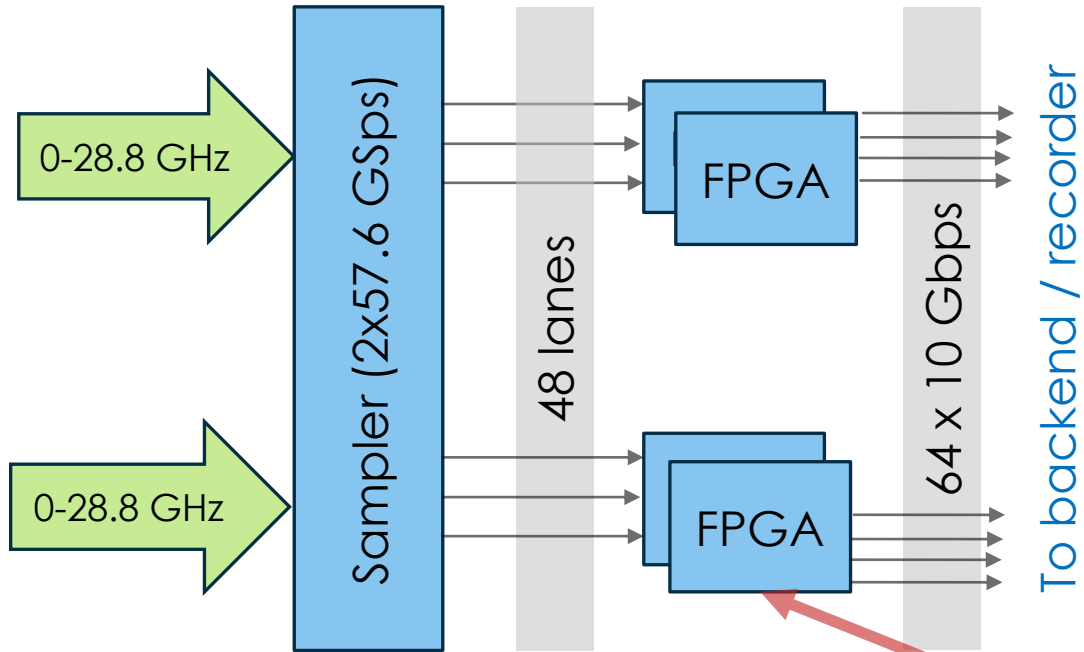
IO

- Input: 2 x 28.8 GHz / 4 x 14.4GHz RFs
- Output: 64 x 10 Gbps (VDIF / raw)

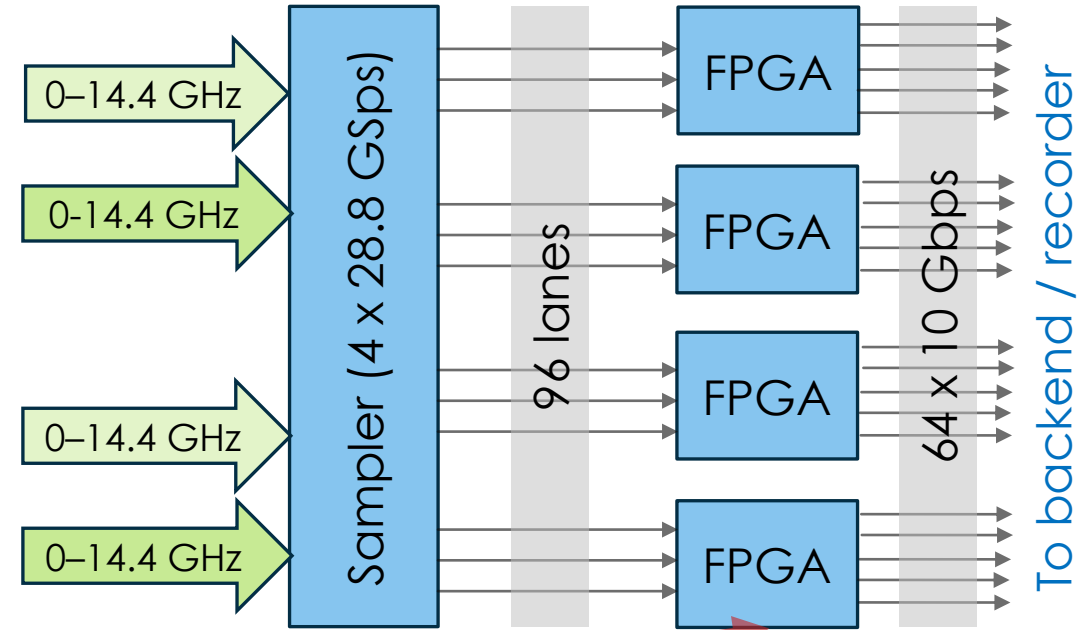
DIFREND28 PROCESSING MODES



Mode 1



Mode 2



Each FPGA provides 4 x 3.6 GHz filtered bands

DIFRENDVGOS

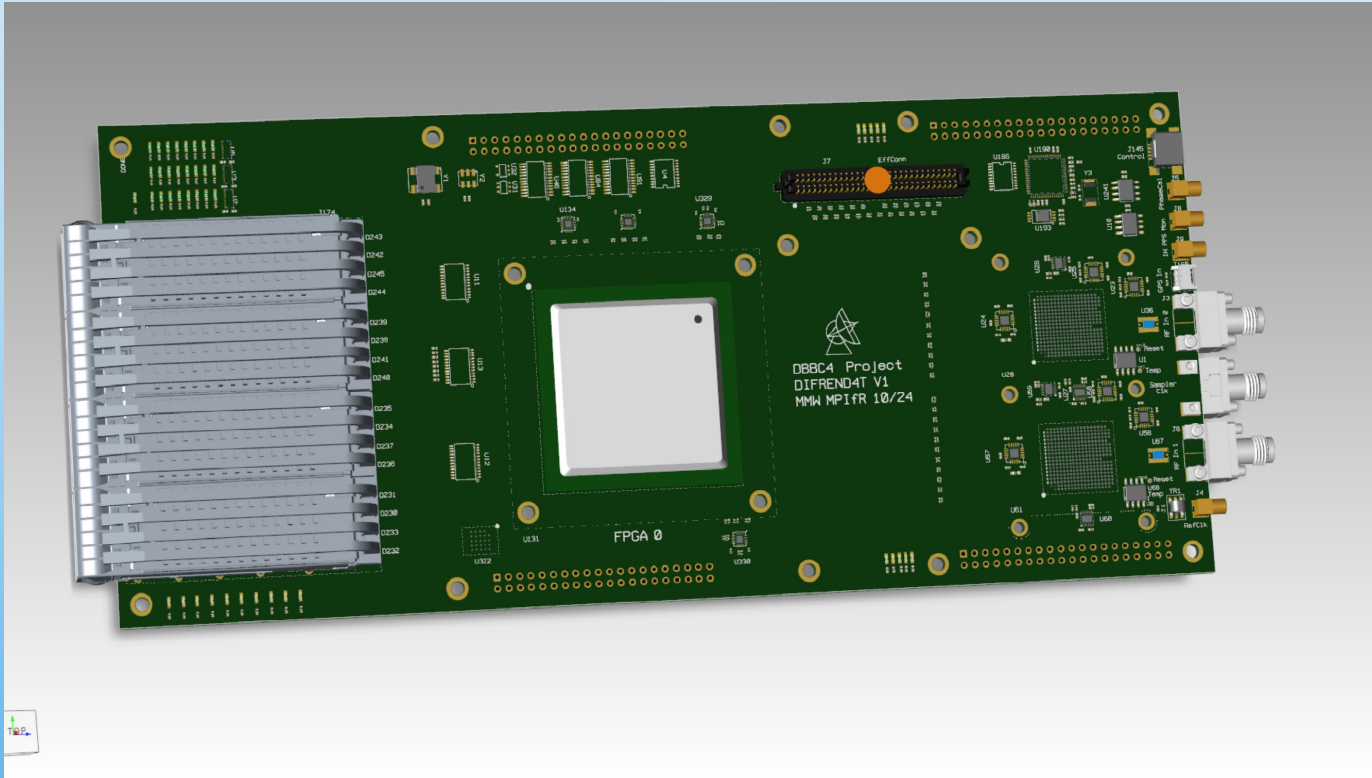


- Based on DIFREND28
- Specially tailored to VGOS observations
 - 14 GHz input band width (VGOS band 2 – 14 GHz)
 - Will provide tunable BBCs with different sub-band widths e.g. 64 MHz, 128 MHz



Status: under development

DIFREND4T



Status: 1st prototype under development

Sampler chip:
Rate: 12.8 Gsps @10 bit
RF range: 0-40 GHz

- Max. input bandwidth:
 - 1 x 0-40 GHz
- Max. output bandwidth:
 - 1 x 6.4 GHz
- Output data rate:
 - 64 Gbps
- VDIF formatting

APPLICATION: BRAND RECEIVER

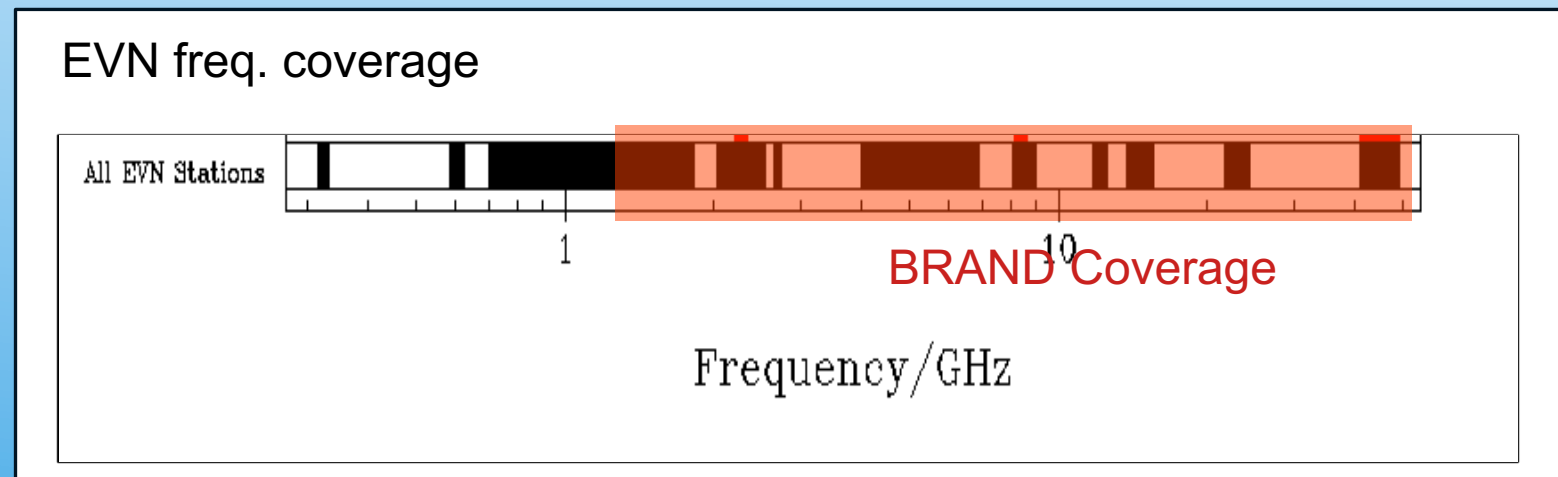


Very-wide band “digital” receiver

- Frequency range: 1.5 - 15.5 GHz
- Instantaneous bandwidth: 14 GHz
- Prototype BRAND receiver for the 100-m telescope (prime focus)

► Targets:

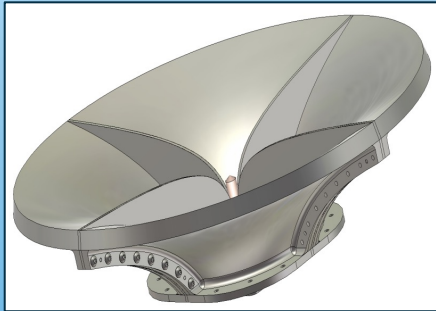
- EVN VLBI array
- VGOS array
- Single dish



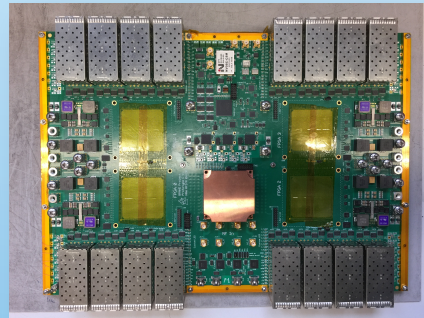
BRAND PROJECT HISTORY



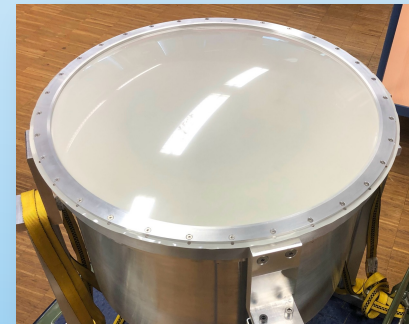
- ▶ Joint Research Activity (JRA) in the Horizon2020 EU funding programme
- ▶ Partners: MPIfR, INAF/Noto, OSO, UAH/IGN, ASTRON, VUC



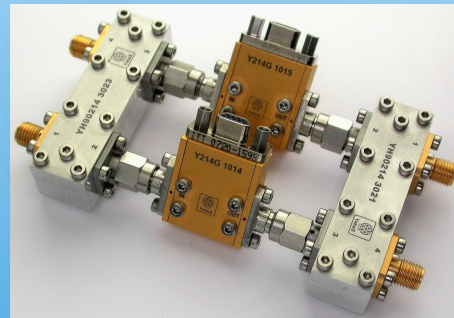
QRFH feed with dielectric inset
Opening angle: 160°
f/D: 0,3
(OSO)



Digital frontend PCB (DiFrEnd28)
Sampling with 2×57.6 Gsps
(MPIfR, INAF/Noto)



Cryostat Window $\varnothing 58$ cm!
With support structure
(MPIfR)



LNA: Balanced amplifier with 2 hybrids and 2 LNAs
(UAH/IGN)

Polarization conversion
With $3\text{dB}/90^\circ$ hybrid
Noise penalty $< 2.5\text{K}$
(UAH/IGN)

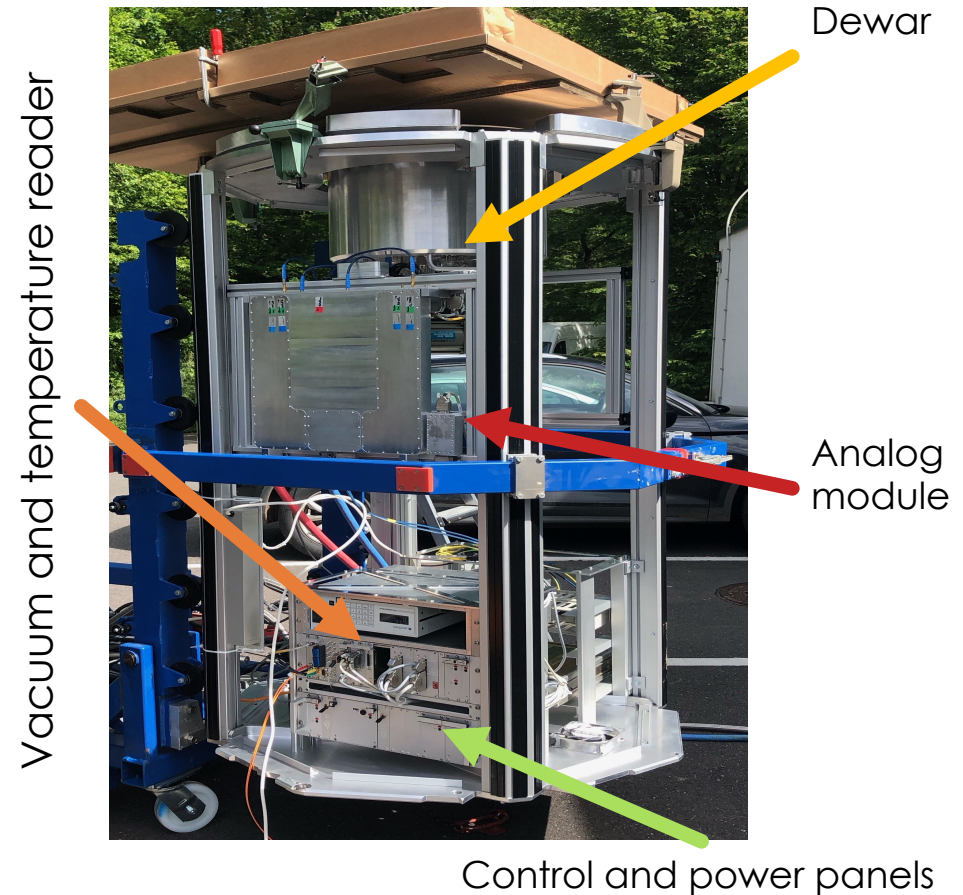
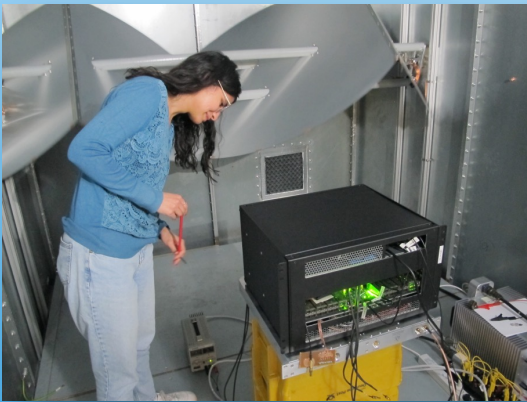


BRAND EFFELSBERG COMMISSIONING



2024

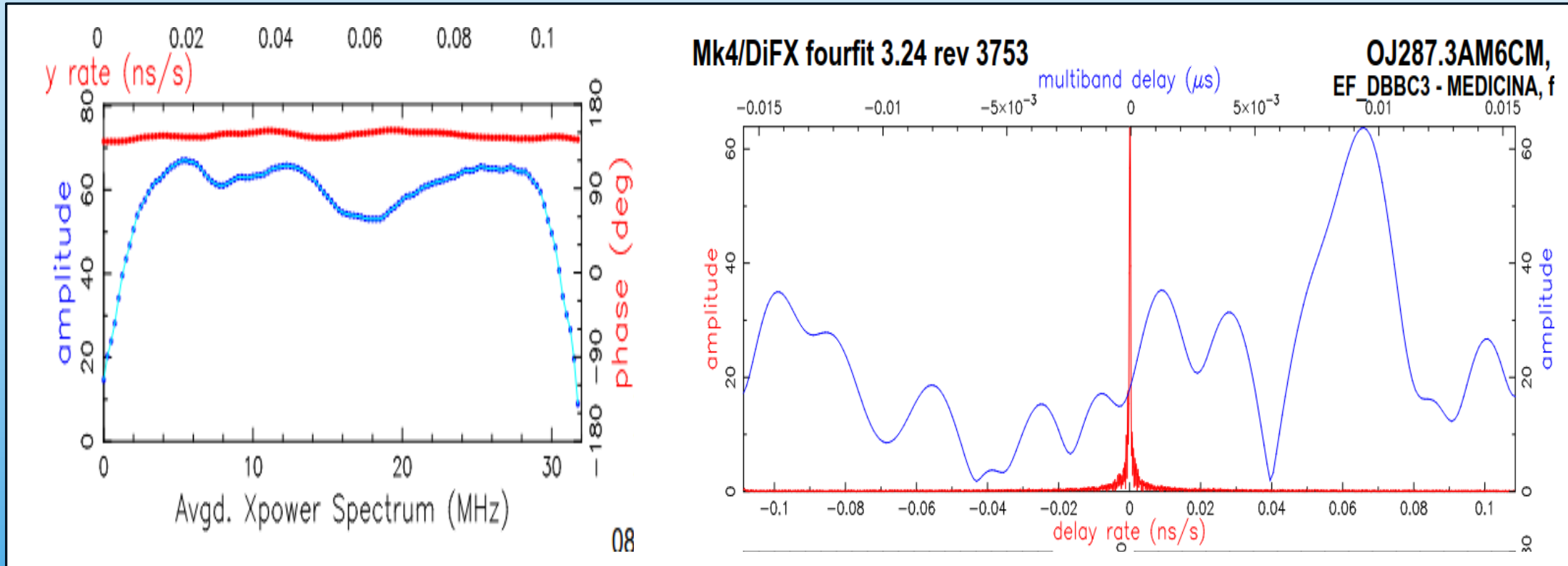
- ▶ Integration of components into full system
- ▶ Lab testing of full system
- ▶ Installation in Effelsberg telescope
- ▶ Final system tests
- ▶ Master thesis by Parisa Rahimi (in preparation)



BRAND FIRST FRINGES



First VLBI Fringes at 4.85 GHz (EVN NME N24C2 with Ef, Mc, On, and Ys)



APPLICATION: DBBC4 BACKEND

The DBBC4^{*)} is the latest of the DBBC family of backends (DBBC, DBBC2, DBBC3)

Technical specs:

- Maximum input bandwidth: $8 \times 28\text{GHz} + 8 \times 4\text{GHz} = \mathbf{256\text{ GHz}}$
- Maximum output data rate: **1 Tbps** @ 2bit sampling

Novel capabilities:

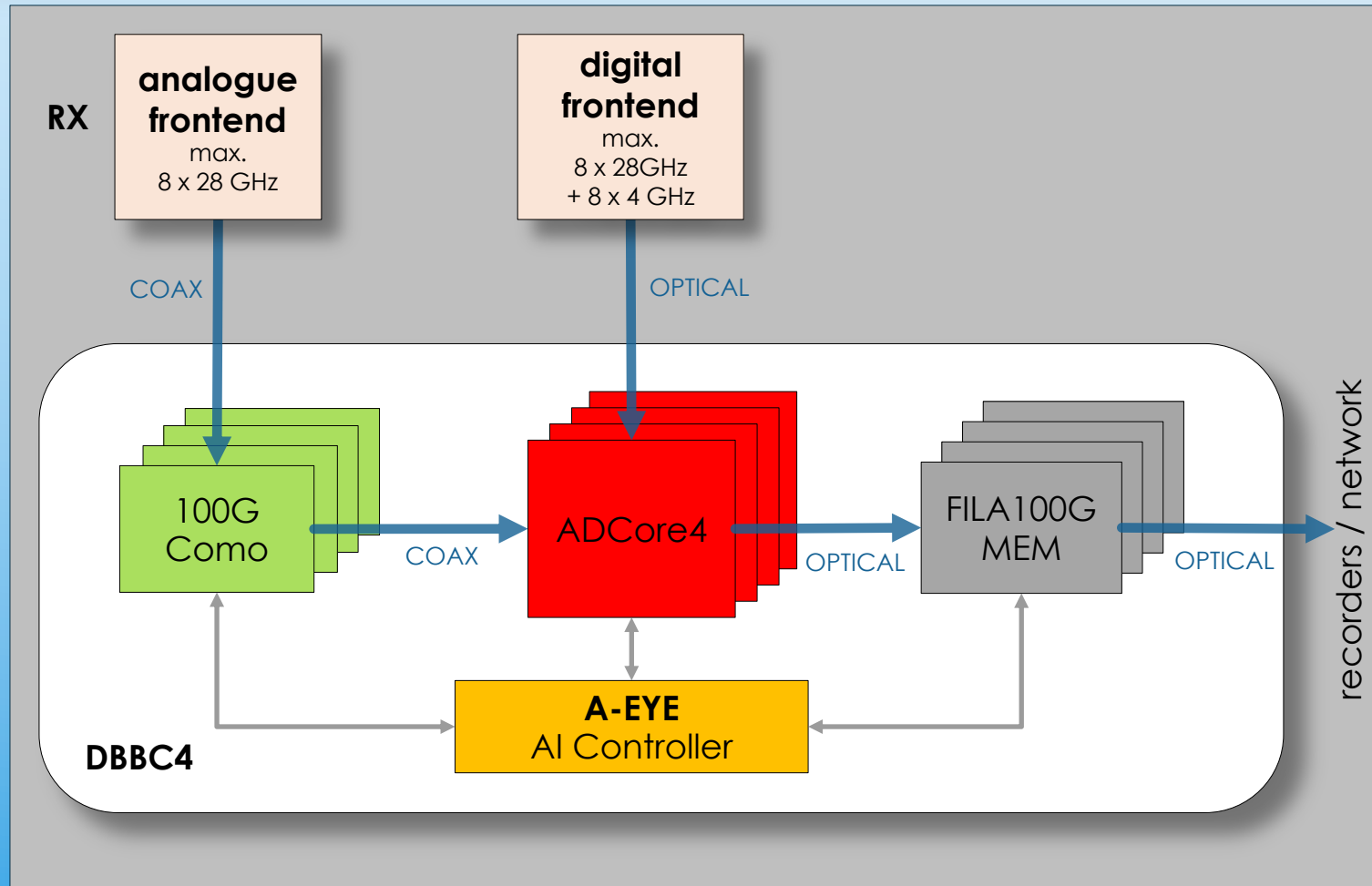
- AI methodology:
 - Real-time interference mitigation
 - Transient search
- Output stream buffering, duplication and modification
 - Burst mode operations (match output data rate to recording rate)
 - Signal streaming to correlators for real-time fringe verification

**) The DBBC4 project has received funding from:*

- the Max Planck Society
- the European Union's Horizon Europe research and innovation programme under grant agreement No 101093934



SYSTEM SCHEMATICS



Modular design:

1 – 4 signal chains

Two operational scenarios*:

1) Analogue-in

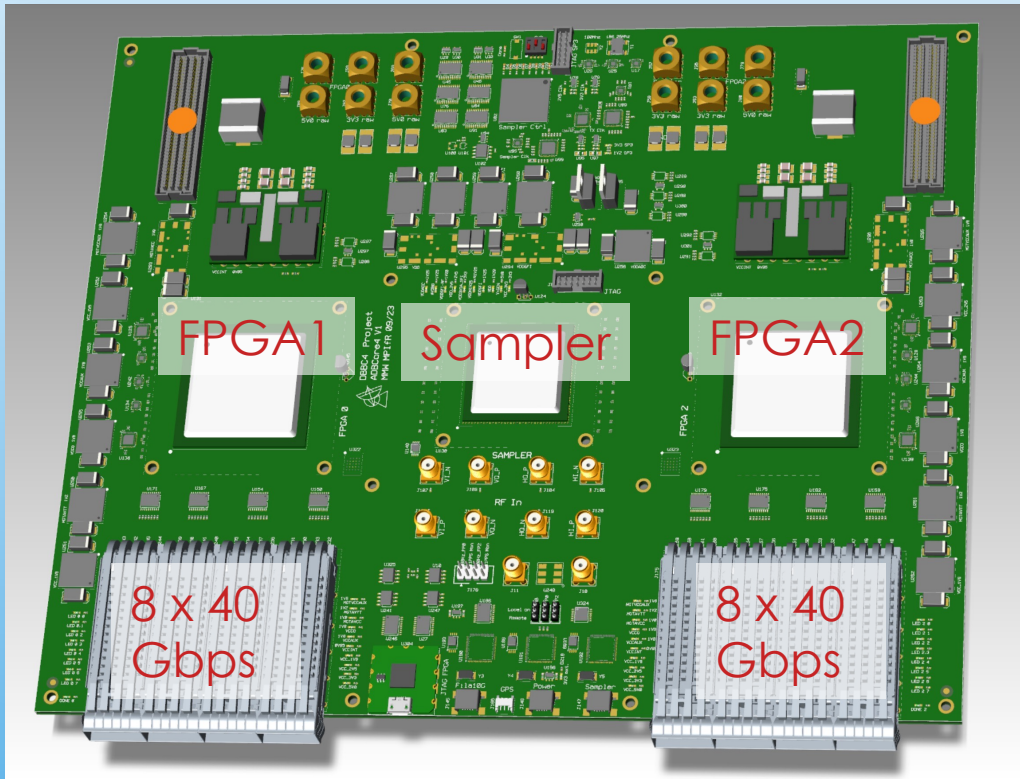
- Sampling of 2 x 28 GHz
- Analogue conditioning

2) Digital-in

- 2 x 28 GHz
- 2 x 4 GHz bw
(in range 0-36 GHz)

* Input bandwidth per signal chain. Max 8x28GHz.

ADCORE4 PCB



- A/D conversion with **2x57.6 Gsps @8bit**
- band processing in various modes
- VDIF formatting

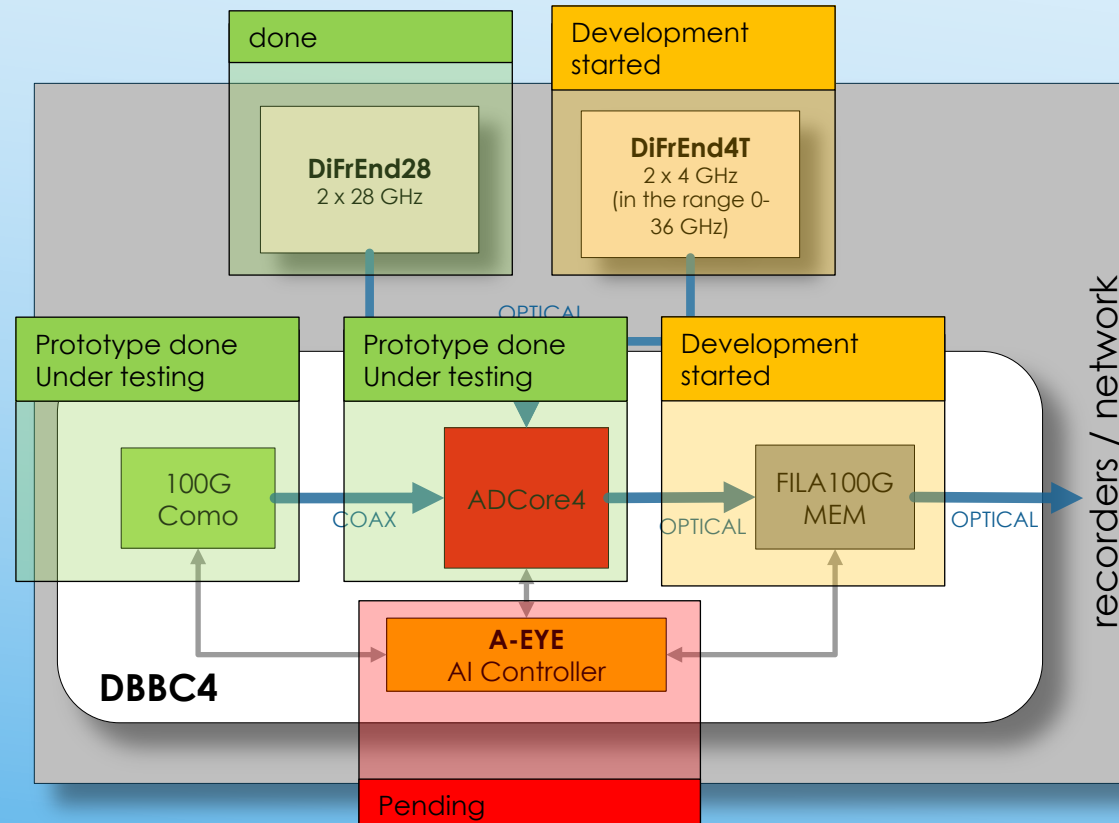
Processing modes

- **DSC**
full 28GHz, direct sampling
- **OCT**
full 28 GHz divided into sub-bands
4 filters of sizes:
225, 450, 900, 1800, 3600, 7200, 14400 MHz
- **DDC**
tunable with sub-bands of various band widths:
3.5, 7, 14, 28.1, 56.25, 112.5 MHz

DBBC4 STATUS AND TIMELINE

- Fully funded by MPG and EC
- Development started early 2023
 - Prototypes have been finished for several components and are currently under testing
 - Firmware/software development is ongoing. Can be adapted from DBBC3 with moderate effort

First functional prototype system is expected to be available in **2025**





Thank you!
Any questions?