DBBC4 PROJECT

A NEXT GENERATION VLBI BACKEND

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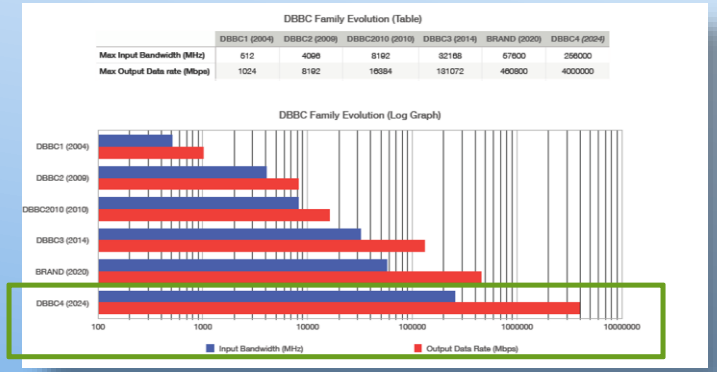
on behalf of the DBBC4 development team

DBBC4 OVERVIEW & SPECS

The DBBC4 is the latest of the DBBC family of backends (DBBC, DBBC2, DBBC3)

Technical specs:

- **Maximum input bandwidth: 8x28GHz + 8x4GHz= 256 GHz**
- **Maximum output data rate: 1 Tbps @ 2bit sampling**



Novel capabilities:

- **AI methodology:**
  - **Real-time interference mitigation**
  - **Transient search**
  - **…….**
- **Output stream buffering, duplication and modification**
  - **Burst mode operations**
  - **Signal streaming to correlators for real-time fringe verification**

DBBC4 DESIGN GOALS

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Future proof approach

- Wide band RX / frequency agility
- Interference mitigation
- Matching of high output data rate to lower recording rates (burst mode)
- Support analogue or digital input signals

Scalability

- Modular design of 1 - 4 dual-polarization signal chains (max. 8 IFs)

Versatility

- Support VGOS, EHT, GMVA, EVN, legacy geodesy observing modes

Compatibility

- Downwards compatible with DBBC3

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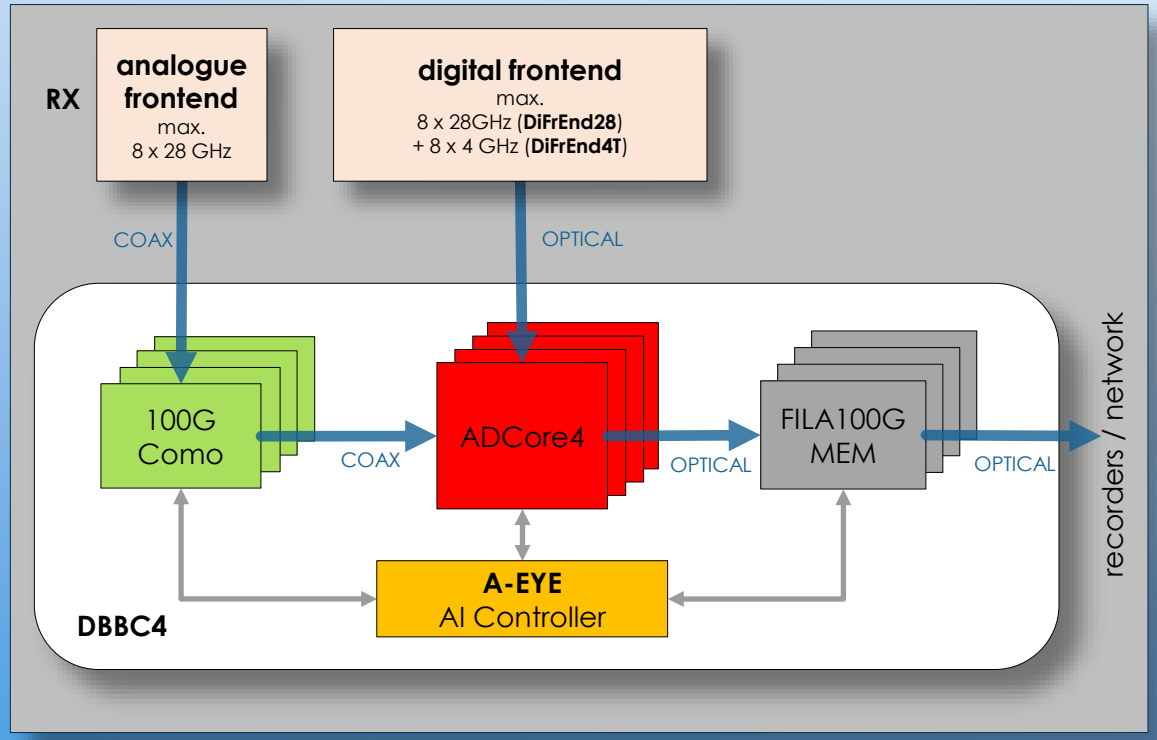
SYSTEM ARCHITECTURE



Modular design:
2 – 8 signal chains

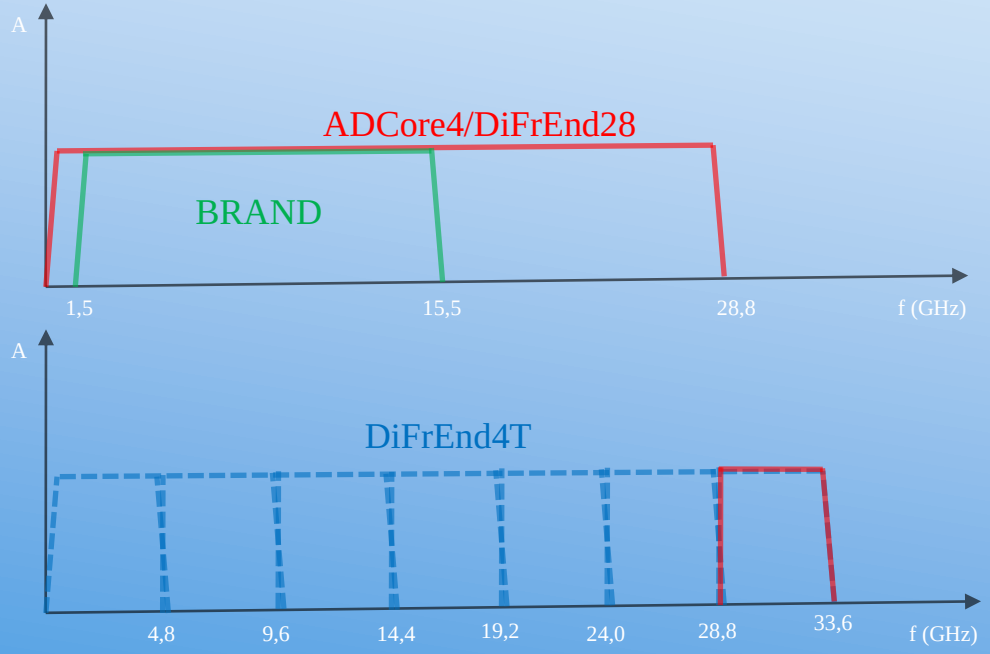
Two operational scenarios*:

1) **Analogue-in**
   - Sampling of 2 x 28 GHz
   - Analogue conditioning

2) **Digital-in**
   - 2 x 28 GHz
   - 2 x 4 GHz bw
     (in range 0-36 GHz)

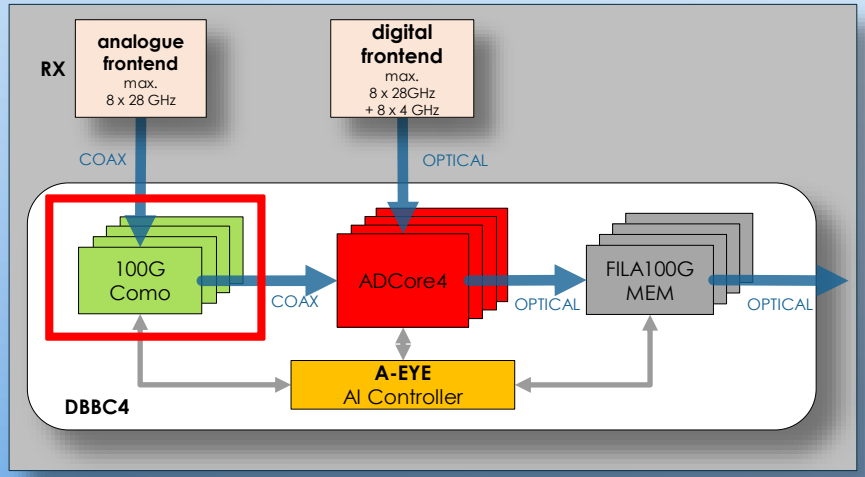
Actual max input bandwidth per signal chain 8x28.8GHz + 8x6 GHz

DBBC4 BAND COVERAGE



- **ADCore4 as standalone sampler and VDIF band forming**
- **DiFrEnd28 as standalone sampler and VDIF band forming**
- **DiFrEnd4T as standalone sampler and VDIF band forming**
- **DiFrEnd28/DiFrEnd4T as sampler and ADCore4 as VDIF band forming for max capabilities**

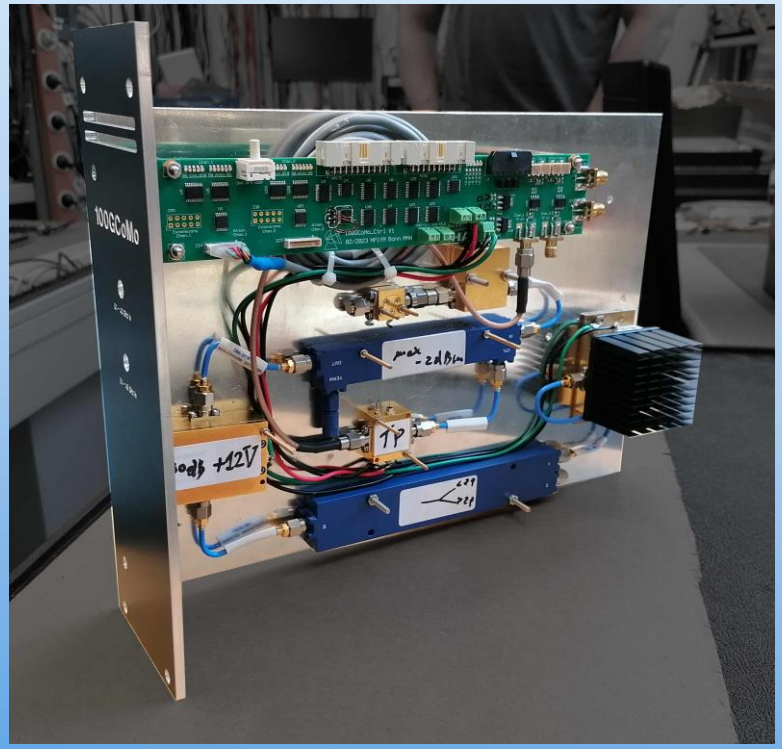
100G COMO



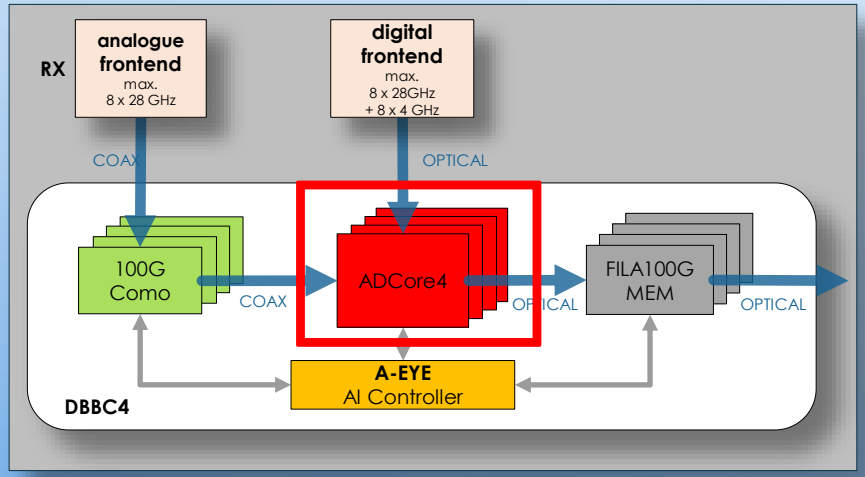
- Analogue conditioning module
- Adapt the analogue input signal for the digital conversion steps in the ADCore4 board.
- Automatic gain control (AGC)
- Measures total power e.g. for Tsys calibration
- Supports Cont_cal noise diode switching for Tsys calibration

- Each 100GComo module processes an input IF band width of 2 x 40 GHz
- A DBBC4 can have up to 4 x 100GComo modules

100GCOMO PROTOTYPE



ADCORE4

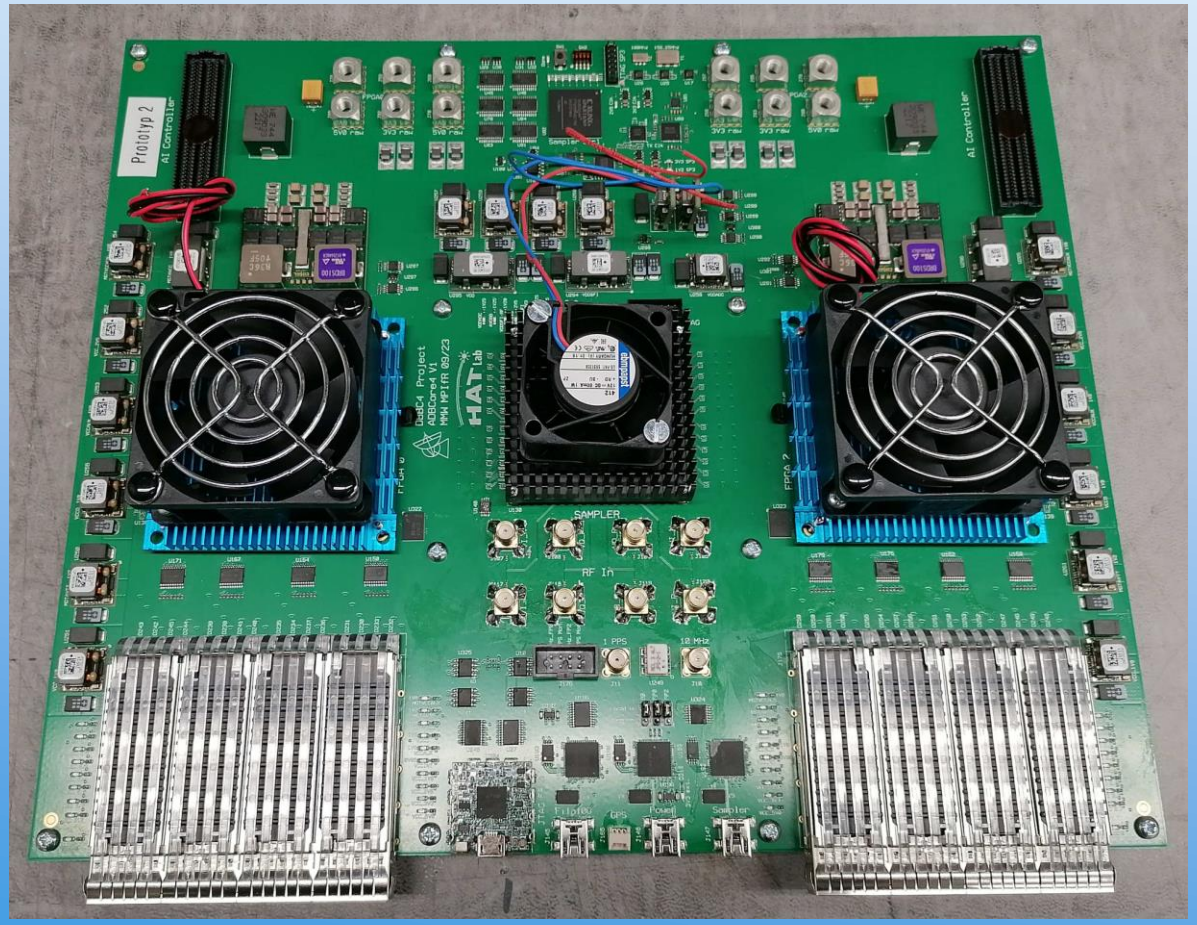


- **A/D conversion with 2x56 Gsps @8bit**
- **and processing in various modes**
- **VDIF formatting**

Processing modes

- **DSC**
  full 28GHz, direct sampling
- **OCT**
  full 28 GHz divided into sub-bands
  4 filters of sizes:
  225, 450, 900, 1800, 3600, 7200, 14400 MHz
- **DDC**
  tunable with sub-bands of various band widths:
  3.5, 7, 14, 28, 56, 112 MHz

ADCORE4


Prototyp 2
AI Controller
AI Controller
SAMPLER
RF In
1 PPS
10 MHz
FPGA 2
HAT lab

DIFREND28 / DIFREND_VGOS DIFREND4T

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Digital frontend components to support "digital-in" mode

- Devices usable also as stand-alone parts
- Required when analogue transport of broad band IFs is not possible /wanted

DiFrEnd28

- Input bandwidth: 2 x 28 GHz
- Sampling at 2x57.6 Gsps @8bit
- Max output data rate: 96 lanes@11.2Gbps = 1Tbps
- DSC, OCT, DDC band forming, output VDIF format

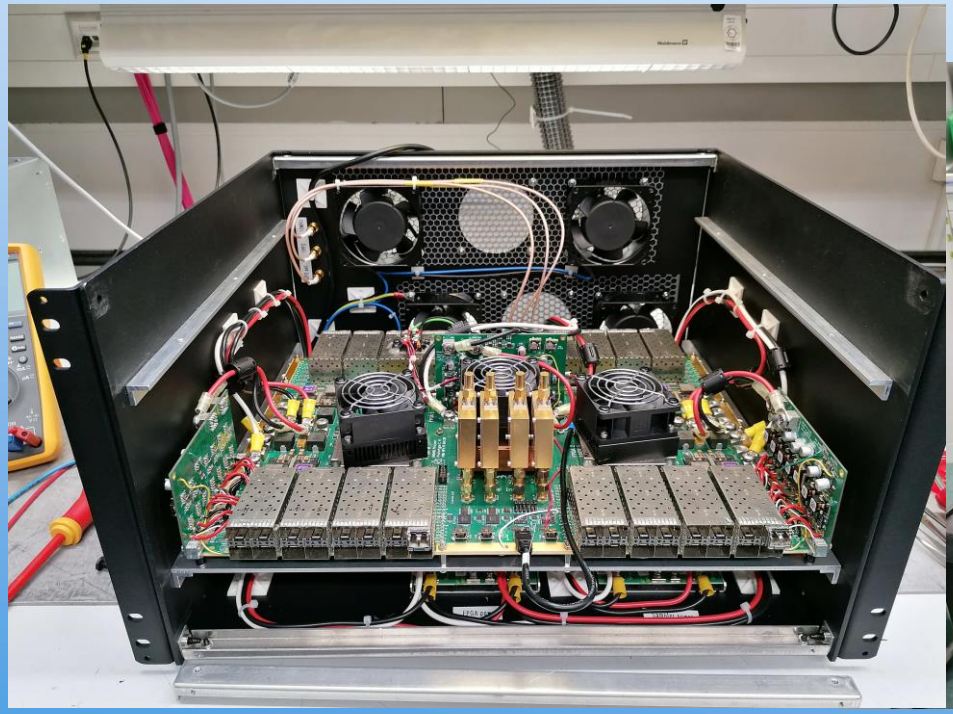
DiFrEnd4T

- Input bandwidth: 2 x 4-6 GHz band width (in the range 0-36 GHz)
- Sampling rate 2 x 8-12 Gsps @ 12bit
- Max output data rate: 288 Gbps
- DSC, OCT, DDC band forming, output VDIF format
- Optical QSFP28 multiple100GE

DiFrEnd_VGOS

- Input bandwidth: 2 x 14.4 GHz
- Sampling at 2x28.8 Gsps @8bit
- Max sampler output data rate: 48 lanes@11.2Gbps = 0.5Tbps
- DSC, OCT, DDC band forming, output VDIF format → to DBBC3 / recorder

DIFREND28 / DIFREND_VGOS PROTOTYPE



DIFREND_VGOS USED WITH DBBC3

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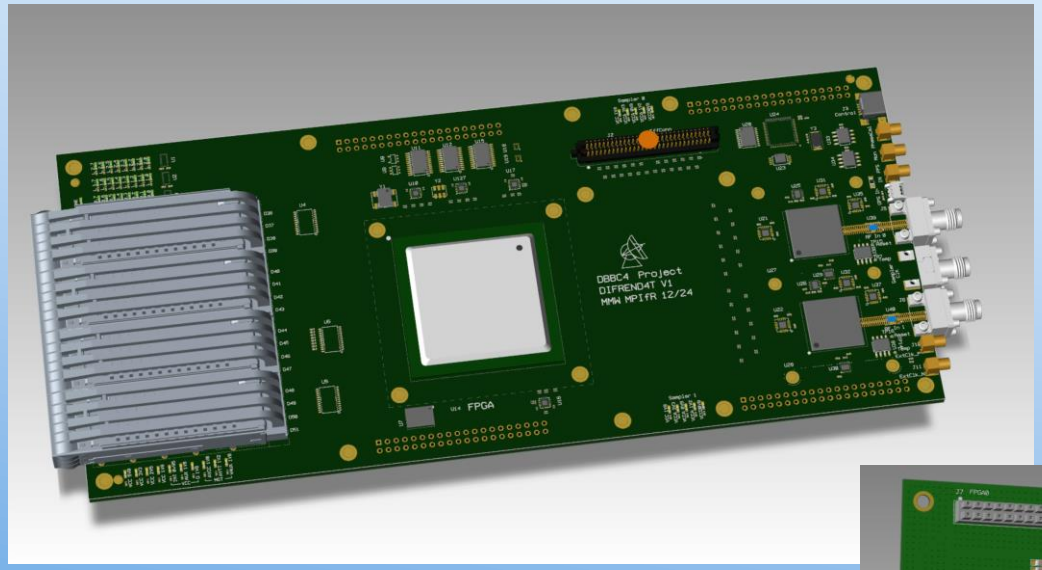
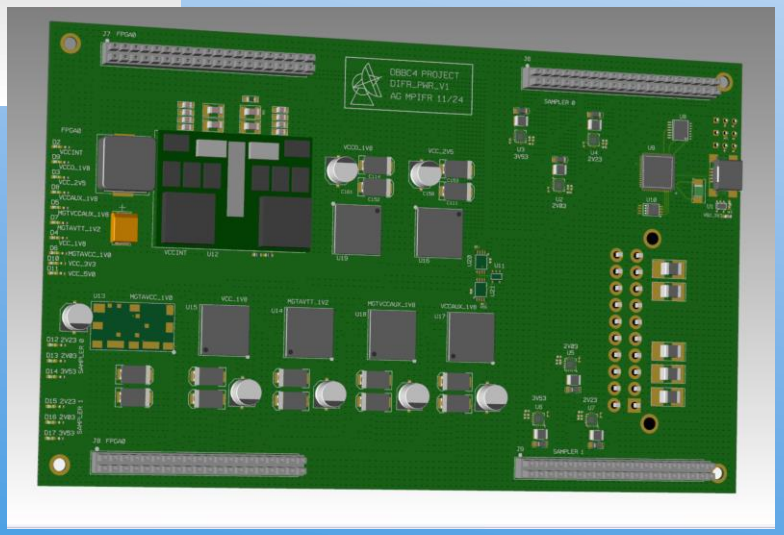
DIFREND4T PROTOTYPE





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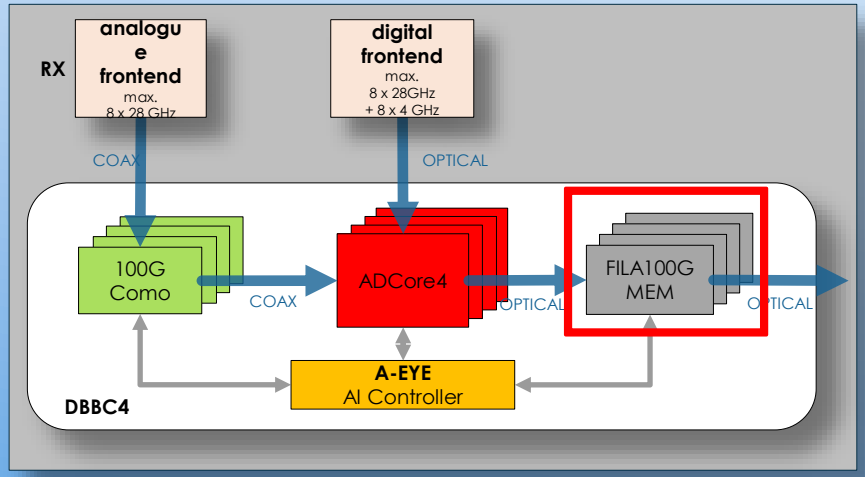
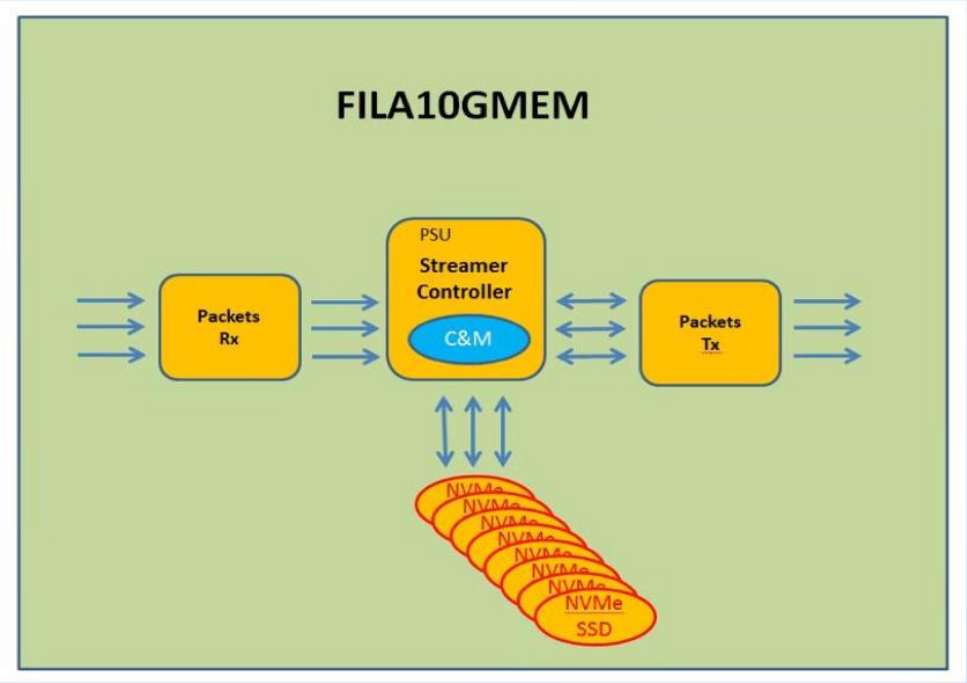
FILA100G MEM



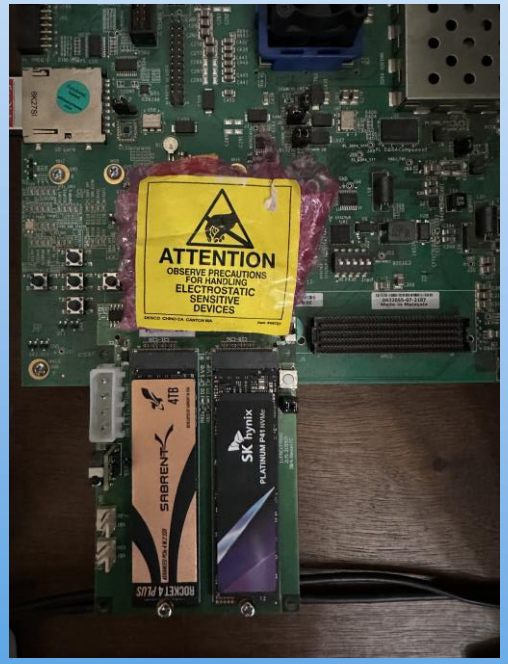
- Fast buffered memory for storage of output streams
- Fast recording onto NVMe/SSD
- Burst-mode recording
- Output stream duplication e.g. for real-time fringe verification at correlators
- Stream manipulation: re-ordering and extraction of channels

FILA100GMEM SCHEMATICS



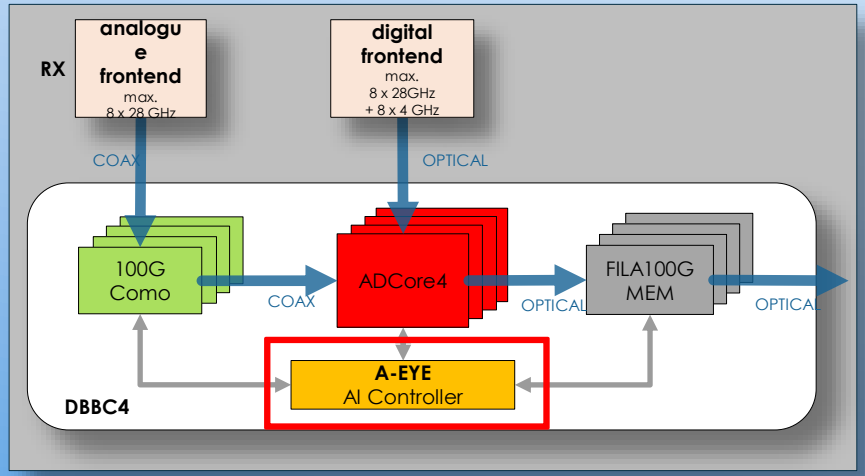
- In/Out Ports + Stream controller for channel manipulation / reordering
- A Slice can accommodate 4 NVMe SSD (currently max 8 TB each)
- A Module can accommodate a up to 4 Slices (currently 128 TB)
- A Unit can accommodate 8 Modules (currently 1024 TB)

FILA100GMEM PRE-PROTOTYPE



- Prototype Board under development
- A number of write/read test under way with several NVMe-SSD
- Burst-mode recording performance (max 80 sec.): 56 Gbps/SSD, 224Gbps/Slice
- Sustained sequential recording performance:
  13 Gbps/SSD, 52 Gbps/Slice
  Current recorder: 16 Gbps

A-EYE CONTROLLER (WP 3.2.3)



Implements artificial intelligence (AI) methodology for e.g.:

- RFI recognition and mitigation
- Extraction of non-statistical noise signals (transient search)
- multi-CPU FPGA device
- synthesizes pre-trained neural networks in a hardware/software DNN (deep neural network).
- interfaces to other DBBC4 components

•A number of possible real-time applications:-

- RFI mitigation
- Pulsar detection
- Fast Radio Burst detection
- Radio anomaly detection
- ... and more

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A-EYE CONTROLLER PRE-PROTOTYPE

- Hardware implementation for a number of neural layer types
- Software implementation for a number of neural layer types
- Combination of harware and software implementation in SystemOnChip (SoC) devices
- Pre-trained networks synthesized for real time applications
- A-EYE prototype board under development
- Three preliminary AI implementation under development

DBBC4 - RADIOBLOCKS PROJECT

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A DBBC4 demonstrator will be realized within the RadioBlocks project

Months 48, started March 2023

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Thanks for your attention

Any questions?

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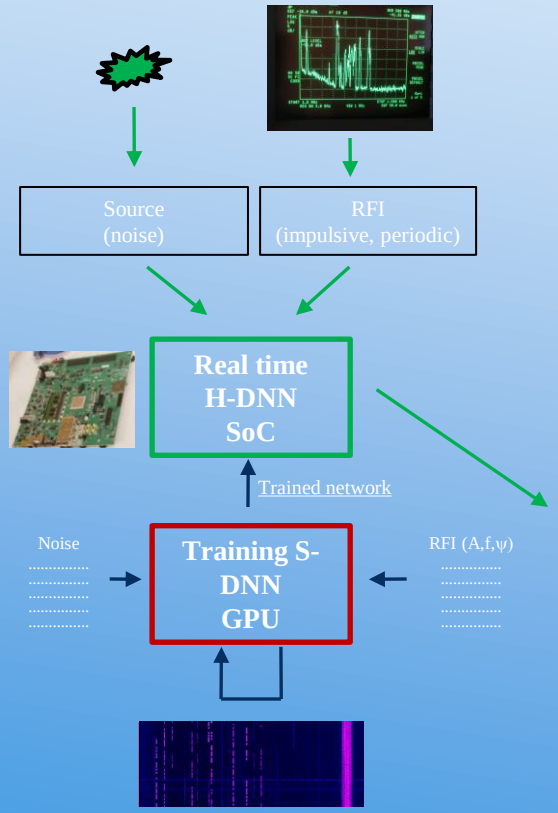
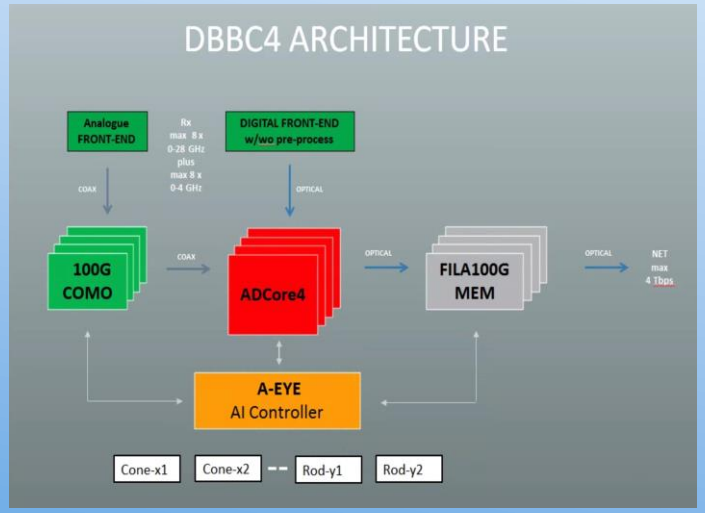
RFI AI-APP IN DBBC4 FOR PULSES





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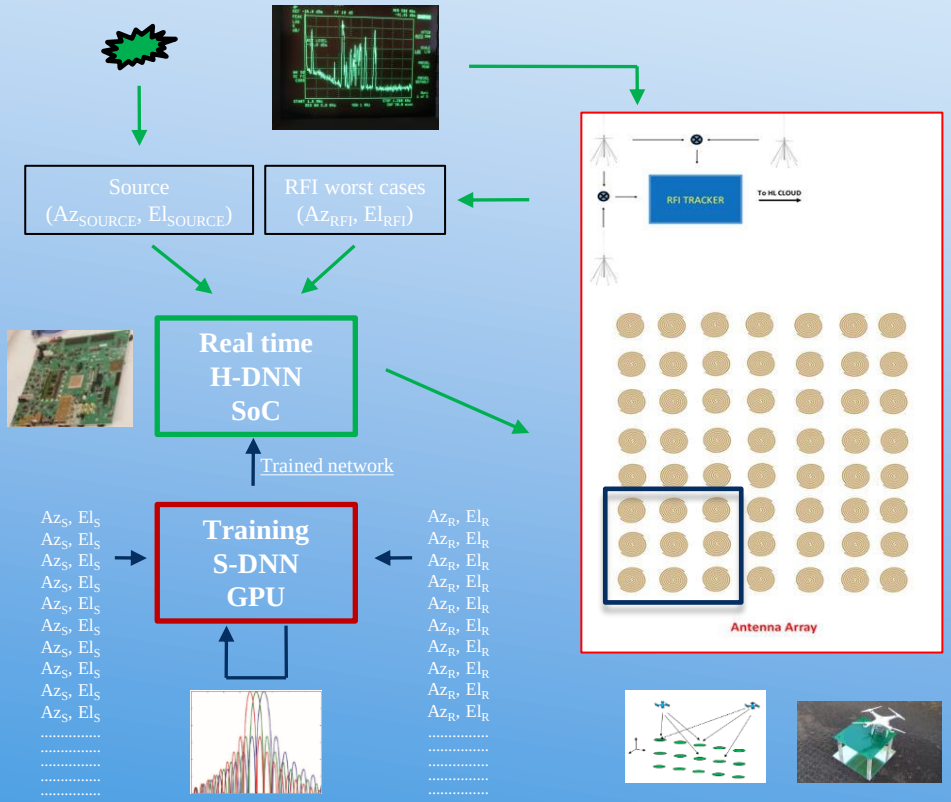
RFI AI-APP IN DBBC4 FOR PHASED ARRAYS



- Pre-trained network for RFI mitigation
- Adaptive beam forming
- Real time RFI tracking
- Multi-direction minimum pointing