

Setup and Operations of the DBBC3

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Max-Planck-Institut
für Radioastronomie



MAX-PLANCK-GESELLSCHAFT

Content

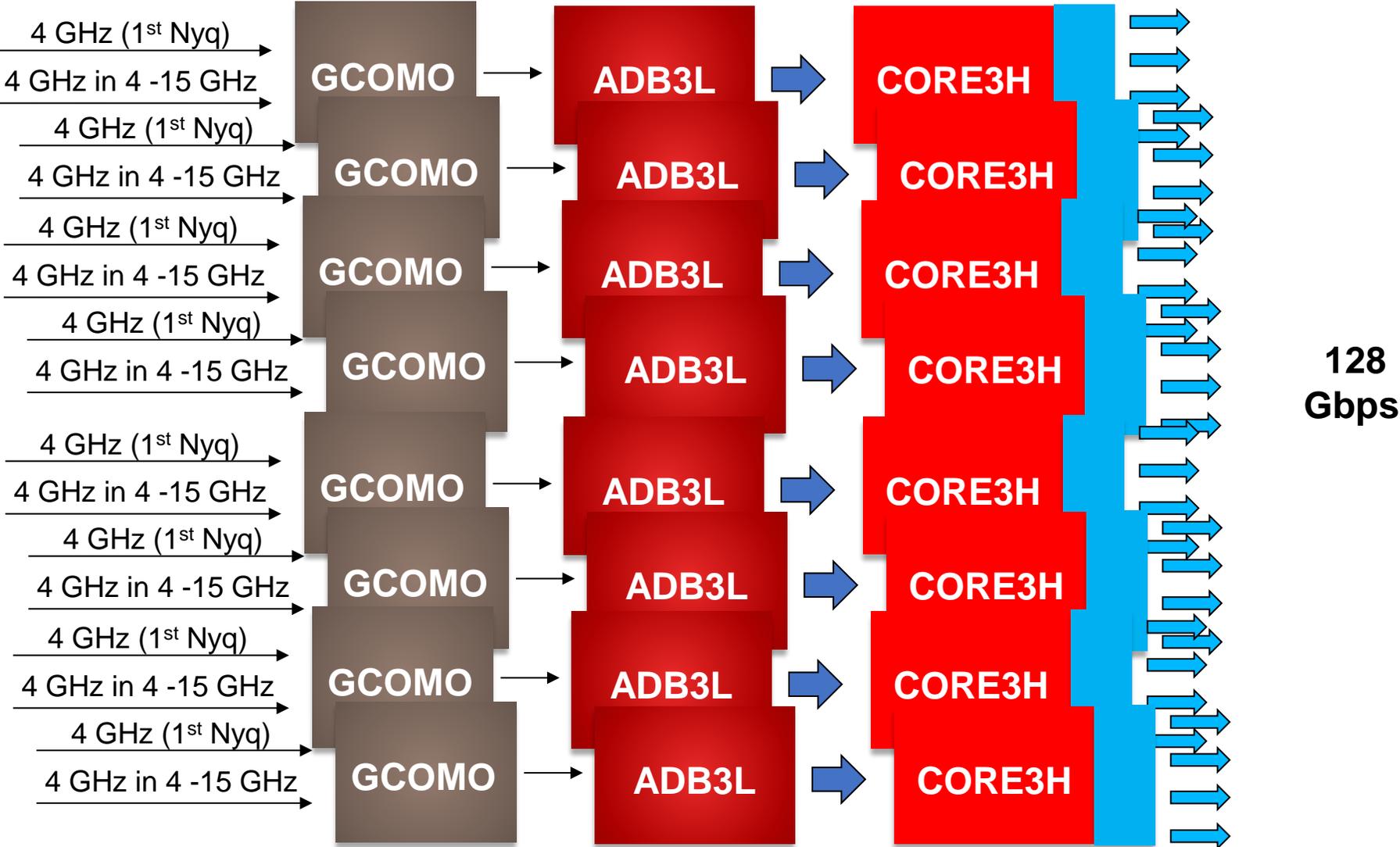
- Introduction and Architecture of the DBBC3
- Observation Modes
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 - Preparations
 - Hardware Connections
 - Software Components
 - Configuration Files
 - Startup Routine
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Introduction

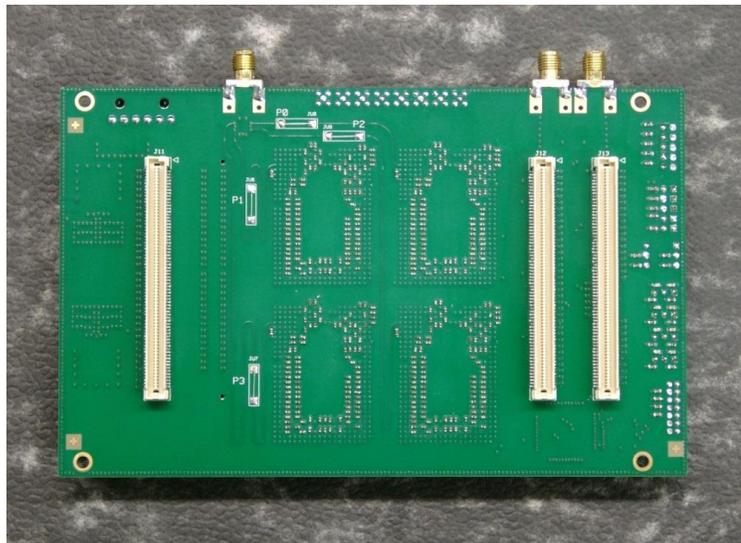


- DBBC3
 - Digital BaseBand Converter for VLBI observations
 - with 2/4/6 or 8 IFs (4096 Mhz input bandwidth each)
 - Output using 4x10Gbit Ethernet/IF with a total output datarate (for 8IF system) of up to 128 Gbps
 - VDIF standard
 - 3 Observation Modes:
 - DSC
 - OCT
 - DDC
 - Evolution of Radionet3 JRA project DBBC3 dedicated to:
 - Astronomy:
 - EVN wide-band VLBI backend
 - mmVLBA network
 - EHT (Event Horizon Telescope)
 - Geodesy:
 - VGOS broad-band VLBI system
 - Partner:
 - INAF – Italy
 - MPIfR – Germany
 - OSO – Sweden

DBBC3 Architecture

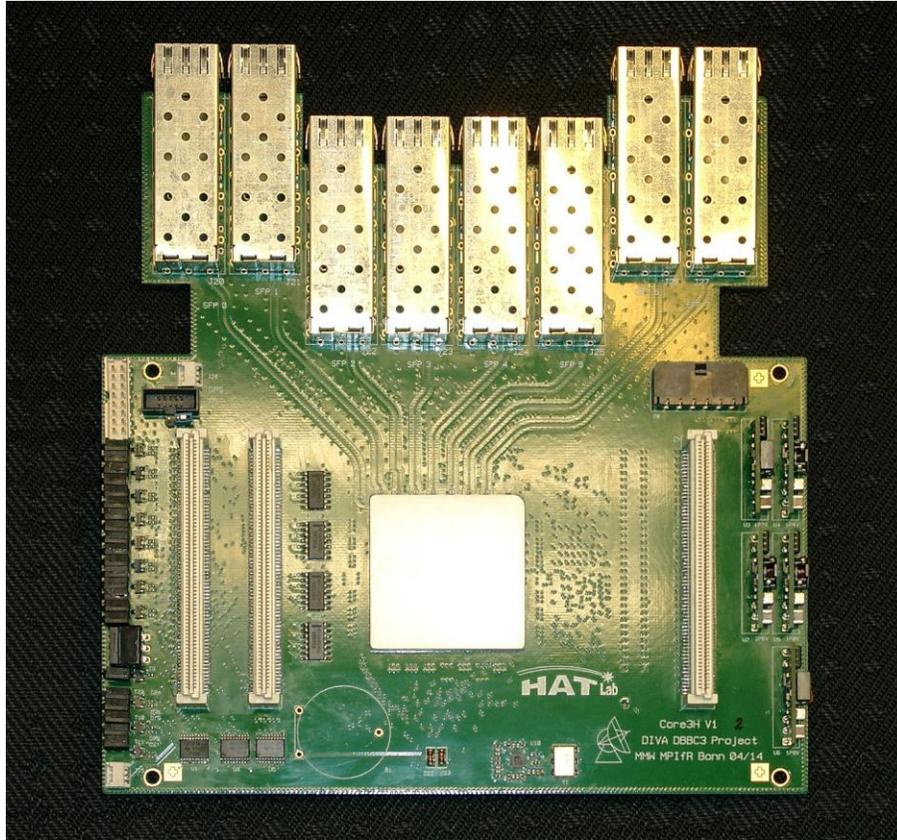


DBBC3 Architecture – ADB3L



- Analog to Digital Converter using interleaved sampling technique with 4 ADCs/Board.
- each ADC runs at 2048 MHz
-> 8 GSps equivalent sample rate
- interleaved sampling requires calibration of:
 - gain
 - offset
 - delay

DBBC3 Architecture – Core3H

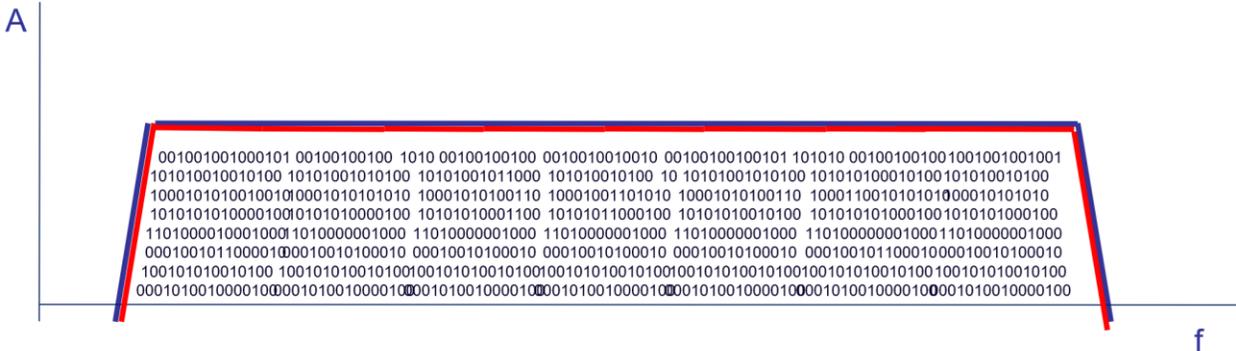


- digital post-processing unit
 - digital filtering (DSC, OCT, DDC)
 - formatting and time synchronization of data stream
 - output VDIF-packets via 10GBit Ethernet
 - up to 8 (default 4) 10GBit Ethernet SFP+ units

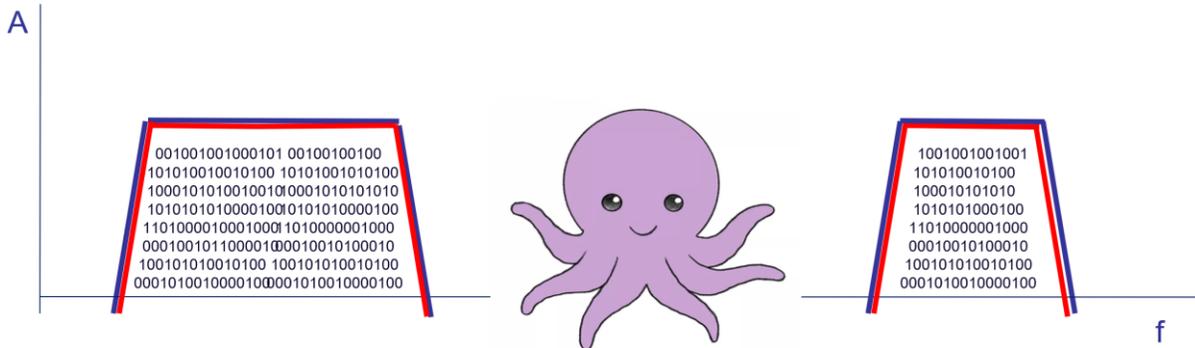
Observation Modes

Observation Modes - DSC

- Direct Sampling Conversion
- 4GHz (4096 MHz) Bandwidth/IF
- Produces four 4Gbit/s streams per IF (interleaved mode)
- Recombination of recorded streams required

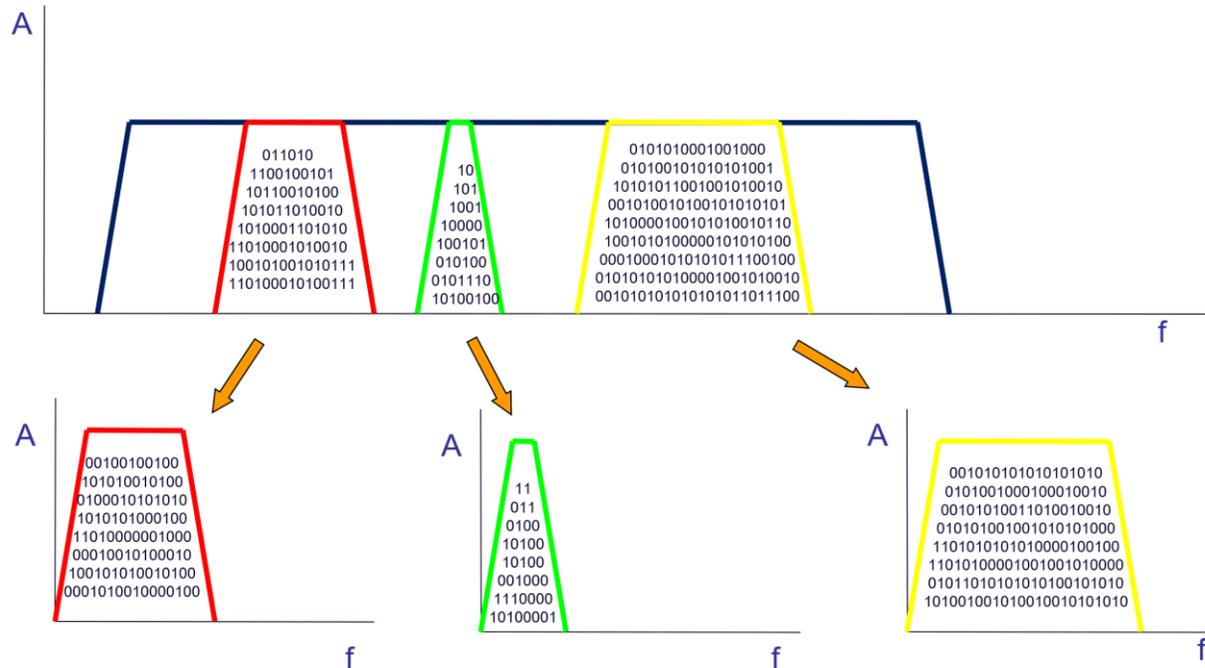


Observation Modes - OCT



- (OCT)opus Mode
- 2 parallel FIR-Filters/IF
- Bandwidth of 256/512/1024/2048 MHz for each Filter
- Produces two output streams with up to 8Gbit/s each
- compatible with 2x2048 MHz/IF observation mode for EHT

Observation Modes - DDC



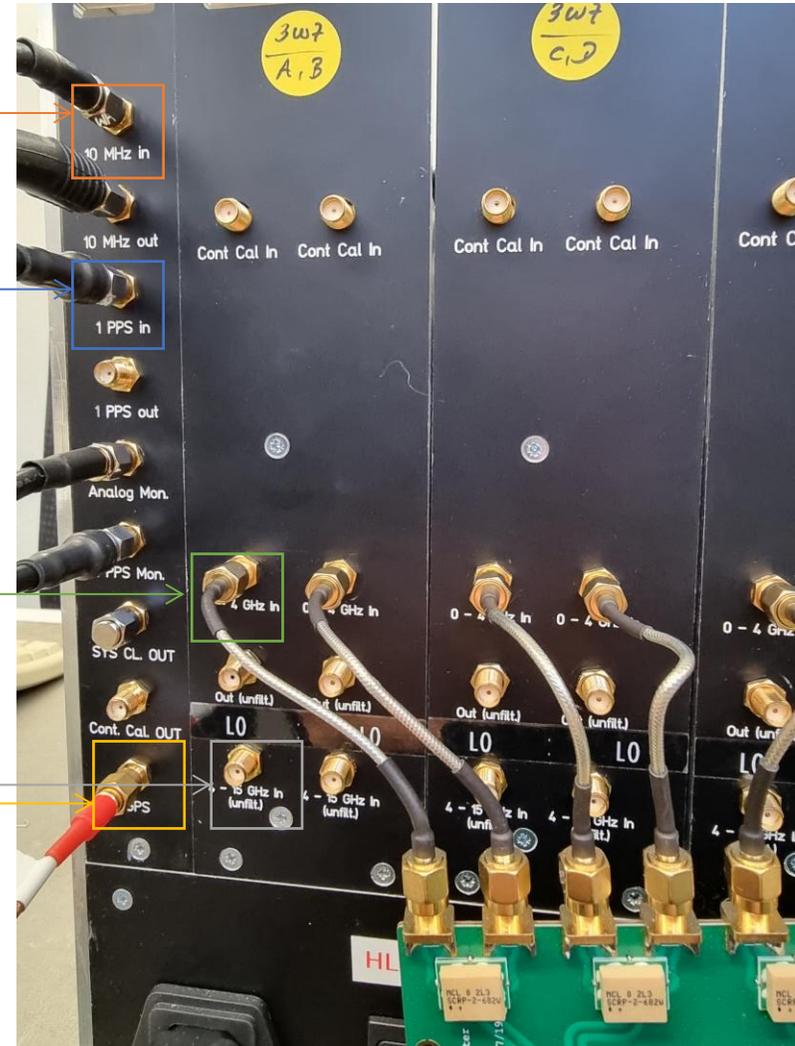
- **Digital DownConversion** typically between high data rate sampled IF band and lower data rate base band
 - Each IF (Core3H) has multiple BBCs (**BaseBand Converter**), that each can be individually tuned to any position within the 4GHz input band with kHz resolution. Each BBC provides two output channels, the upper and lower sideband (USB/LSB), and has its own automatic gain control.
- **DDC_V: (VGOS)**
 - Latest version: v126 (2024)
 - 16 tunable BBCs/IF with upper/lower sideband each
 - v125 and lower had 8 BBCs/IF
 - Fixed 32 MHz BW/sideband with specialized filters
- **DDC_U (Universal)**
 - Latest version: v127 (2024)
 - Test version: v130 (beta) with simplified setup routine
 - 16 tunable BBCs/IF with upper/lower sideband each
 - Selectable 2, 4, 8, 16, 32, 64, 128 MHz BW/sideband
 - 8 bit mode support since v127
- **DDC_E (EVN)**
 - Latest version: v128 (2025)
 - 8 tunable BBCs/IF with upper/lower sideband each
 - Selectable 2, 4, 8, 16, 32, 64, 128 MHz BW/sideband with improved filters
 - 8 bit mode support since v127

Preparations

Hardware Connections

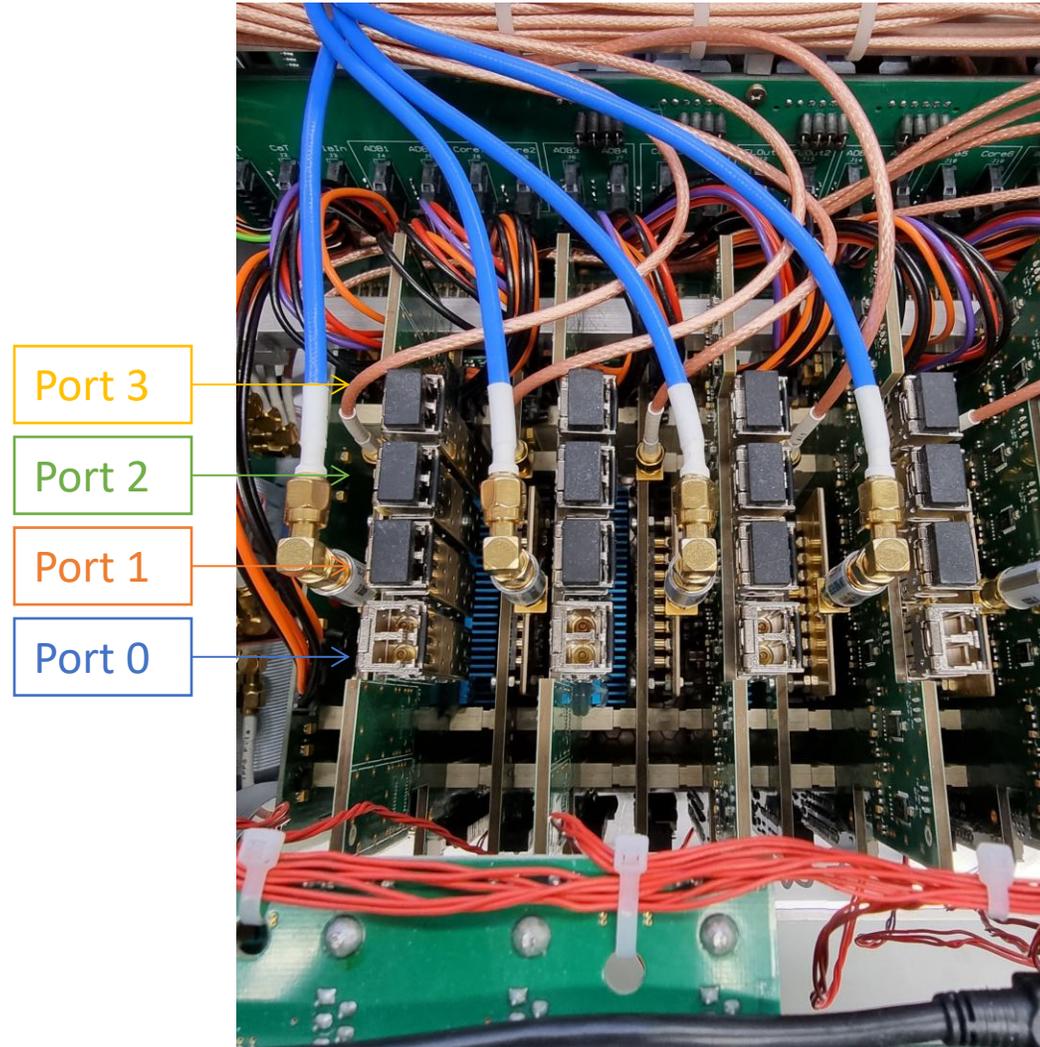
- Necessary Connections on the Back:

- 10 MHz
- 1 PPS
- GPS
- Signal Input 0-4 GHz
- Or Signal Input 4-15 GHz
 - with down-conversion
 - Connect "Out (unfilt.)" to "0-4 GHz in"



Hardware Connections

- Ethernet Output:
 - 4 Ethernet Ports/IF
 - Extension to 8 ports/IF possible.
 - DDC_V/E: Port 0
 - DDC_U: Port 0 and 1
 - First block of 8 BBCs: Port 0
 - Second block of 8 BBCs: Port 1
 - OCT: Port 0 and 2
 - Filter 1 Port 0 (copy to Port 1)
 - Filter 2 Port 2 (copy to Port 3)
 - DSC: Port 0-3



Software Components

- Control Software
- Client
- Firmware
- Configuration Files
- Python Toolkit for Multicast Monitoring and Remote Control

Software Components

- **Control Software**
 - Client
 - Firmware
 - Configuration Files
 - Python Toolkit
- Located in C:\DBBC\bin folder
 - One exe-File for each Observation Mode:
 - DBBC3 Control DSC_v120.exe
 - DBBC3 Control OCT_D_v120.exe
 - DBBC3 Control DDC_V_v126.exe
 - ...
 - Link to each File on Desktop

Software Components

- Control Software
- **Client**
- Firmware
- Configuration Files
- Python Toolkit
- Located in C:\DBBC\bin folder
- DBBC client v4.exe
- Local Client used to communicate with Control Software
- Link on Desktop

Software Components

- Control Software
 - Client
 - **Firmware**
 - Configuration Files
 - Python Toolkit
- Located in C:\DBBC_CONF\FilesDBBC folder
 - One bit-File for each Observation Mode:
 - dbbc3_dsc_2hv2_221122.bit
 - dbbc3_oct_D_2hv2_221122.bit
 - DDC_V-2hv2_16bbc_200324.bit
 - ...

Software Components

- Control Software
 - Client
 - Firmware
 - **Configuration Files**
 - Python Toolkit
- Located in C:\DBBC_CONF folder
 - C:\DBBC_CONF\DSC_120 for DSC Mode
 - C:\DBBC_CONF\OCT_D_120 for OCT_D Mode
 - C:\DBBC_CONF for DDC versions (before v130)
 - C:\DBBC_CONF for config_adb3l.txt
 - Five types of configuration files
 - Main config file
 - Sampler config file
 - Core3H config files (one for each IF)
 - BBC config file (for DDC modes)
 - Filter tap files (for OCT_D mode)

Main Config File

- Example: `dbbc3_config_file_ddc_V_126.txt`
- References to other config files
- Init Part for Core3H-Boards
- Init Part for GCoMo-Modules
- Synthesizer Config
- IP-Address of DBBC3
- IP and Port for Multicast Group
- Maximum Number of Phasechecks

```
config_adb3l.txt
config_ddc_V_16BBC.txt
3 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_1.fila10g COM3
3 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_2.fila10g COM4
30 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_3.fila10g COM5
30 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_4.fila10g COM6
0 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_5.fila10g COM7
0 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_6.fila10g COM8
0 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_7.fila10g COM9
0 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_8.fila10g COM10
3 4500 10 32000 COM11
3 4500 10 32000
3 4500 10 32000 COM12
3 4500 10 32000
0 28000
0 28000
0 28000
0 28000
CAT3 2048
134.104.30.223
224.0.0.255:25000
20
```

Main Config File

- Init Part for Core3H-Boards

- Core3H Status:

- 3: Installed Core3H and Signal connected to IF
 - 30: Installed Core3H and NO Signal connected
 - 0: No Installed Core3H

- Core3H Firmware

- Core3H Config File

- Serial COM Port

config_adb3l.txt

config_ddc_V_16BBC.txt

```
3 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_1.fila10g COM3
3 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_2.fila10g COM4
30 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_3.fila10g COM5
30 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_4.fila10g COM6
0 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_5.fila10g COM7
0 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_6.fila10g COM8
0 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_7.fila10g COM9
0 DDC_V-2hv2_16bbc_200324.bit ddc_V_16BBC_core3H_8.fila10g COM10
```

```
3 4500 10 32000 COM11
```

```
3 4500 10 32000
```

```
3 4500 10 32000 COM12
```

```
3 4500 10 32000
```

```
0 28000
```

```
0 28000
```

```
0 28000
```

```
0 28000
```

```
CAT3 2048
```

```
134.104.30.223
```

```
224.0.0.255:25000
```

```
20
```

Main Config File

- Init Part for GCoMo-Modules
 - GCoMo Status:
 - 3: Installed
 - 0: Not Installed
 - Synthesizer Frequency for Down Conversion
 - In MHz
 - ½ of LO-Frequency
 - Attenuation for Synthesizer Frequency
 - in dBm
 - AGC Power Target
 - COM Port for Synthesizer Communication
 - 2 IFs share one Synthesizer (with 2 Outputs each)

```
config_adb3l.txt
config_ddc_U.txt
3 dbbc3_ddc_U_v130-2hv2_180423.bit ddc_E_core3H_1.fila10g COM3
3 dbbc3_ddc_U_v130-2hv2_180423.bit ddc_E_core3H_2.fila10g COM4
30 dbbc3_ddc_U_v130-2hv2_180423.bit ddc_E_core3H_3.fila10g COM5
30 dbbc3_ddc_U_v130-2hv2_180423.bit ddc_E_core3H_4.fila10g COM6
0 dbbc3_ddc_U_v130-2hv2_180423.bit ddc_E_core3H_5.fila10g COM7
0 dbbc3_ddc_U_v130-2hv2_180423.bit ddc_E_core3H_6.fila10g COM8
0 dbbc3_ddc_U_v130-2hv2_180423.bit ddc_E_core3H_7.fila10g COM9
0 dbbc3_ddc_U_v130-2hv2_180423.bit ddc_E_core3H_8.fila10g COM10
3 4500 10 32000 COM11
3 4500 10 32000
3 4500 10 32000 COM12
3 4500 10 32000
0 28000
0 28000
0 28000
0 28000
CAT3 2048
134.104.30.223
224.0.0.255:25000
20
```

Sampler Config File

- Example: adb3l_config.txt

- Static Part

- Do not Change

- Delay, offset and gain for each sampler

- command=board,sampler,value
 - board[1-8]
 - sampler[0-3]
 - Value determined by Calibration Procedure

- Only one file per system, shared by all observation modes!

```
bistoff=1
bistoff=2
reset
SDA_on=1,0
SDA_on=1,1
SDA_on=1,2
SDA_on=1,3
SDA_on=2,0
SDA_on=2,1
SDA_on=2,2
SDA_on=2,3
delay=1,0,266
delay=1,1,454
delay=1,2,570
delay=1,3,758
offset=1,0,136
offset=1,1,123
offset=1,2,121
offset=1,3,105
gain=1,0,142
gain=1,1,104
gain=1,2,122
gain=1,3,150
delay=2,0,59
delay=2,1,375
delay=2,2,649
delay=2,3,729
...
```

Core3H Config Files

- Example: ddc_V_core3H_1.fila10g

```
core3_init
core3_mode pfb
regwrite core3 0 0x15151515
regwrite core3 1 0xBFBFBFBF
regwrite core3 9 1
reboot
inputselect vsi1-2
vsi_samplerate 128000000 2
splitmode off
reset
vdif_frame 2 32 8000 ct=off
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:42:38:e2
destination 0 192.168.1.2:46220
timesync
start vdif
sysstat
```

- Example: oct_D_core3H_1.fila10g

```
reboot
core3_init
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbcfg eth2 ip=192.168.1.18 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:44:47:60
tengbarp eth2 4 00:60:dd:44:0b:8a
destination 0 192.168.1.2:46220
destination 2 192.168.1.4:46222
timesync
start vdif
sysstat
```

Core3H Config Files

- Example: ddc_V_core3H_1.fila10g

```
core3_init
core3_mode pfb
regwrite core3 0 0x15151515
regwrite core3 1 0xBFBFBFBF
regwrite core3 9 1
reboot
inputselect vsi1-2
vsi_samplerate 128000000 2
splitmode off
vsi_bitmask 0x55555555 0x55555555
reset
vdif_frame 2 32 8000 ct=off
```

```
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:42:38:e2
destination 0 192.168.1.2:46220
timesync
start vdif
sysstat
```

- General commands, most of them are fixed for a given observation mode. The exceptions are:
 - For DDC_U/E the **vsi_samplerate**-command is used to adjust the data rate to the selected BBC-bandwidth
 - The **bitmask**-command can be used if you want to select a subset of the channels for output
 - The **vdif_frame**-command is used to configure the VDIF Header information. The parameters are:
 - Bits/Channel (default 2)
 - Number of Channels/VDIF Frame
 - Byte-size /VDIF Frame
 - ct=off should be always off, Corner Turning is not currently supported

Core3H Config Files

- Example: ddc_V_core3H_1.fila10g

```
core3_init
core3_mode pfb
regwrite core3 0 0x15151515
regwrite core3 1 0xBFBFBFBF
regwrite core3 9 1
reboot
inputselect vsi1-2
vsi_samplerate 128000000 2
splitmode off
vsi_bitmask 0x55555555 0x55555555
reset
vdif_frame 2 32 8000 ct=off
tengbcfg eth0 ip=192.168.1.16 gateway=192.168.1.1 nm=27
tengbarp eth0 2 00:60:dd:42:38:e2
destination 0 192.168.1.2:46220
timesync
start vdif
sysstat
```

- Ethernet Configuration:

- The **tengbcfg**-command is used to configure the source parameters of the ethernet ports, like IP-Address, Gateway, Netmask and if needed MAC address
- The **tengbarp**-command is used to configure the ARP table, which allows assigning target MAC addresses to a given port and subnet
- The **destination**-command is used to set the target IP-Address and Port for a given output
 - With the parameter “none” instead of an IP-Address you can also disable the output from this port

BBC Config File

- Initial Configuration for the BBCs:

- BBC Number (1-128)
- Frequency
- Bandwidth

- BBC Numbering for DDC_U and DDC_V (v126+):

Board 1	Board 2	Board 3	Board 4	Board 5	Board 6	Board 7	Board 8
1-8	9-16	17-24	25-32	33-40	41-48	49-56	57-64
65-72	73-80	81-88	89-96	97-104	105-112	113-120	121-128

```
1 300.0 128
2 300.0 128
3 300.0 128
4 300.0 128
5 300.0 128
6 300.0 128
7 300.0 128
8 300.0 128
9 300.0 128
10 300.0 128
11 300.0 128
12 300.0 128
13 300.0 128
14 300.0 128
15 300.0 128
16 300.0 128
10 300.0 128
11 300.0 128
12 300.0 128
13 300.0 128
14 300.0 128
15 300.0 128
16 300.0 128
```

...

Startup Routine

Post-Startup System Check

Post-Startup System Check

1. Check GCoMo Power Levels
2. Phasecheck
3. Check PPS Synchronization
4. Check Time Synchronization

Post-Startup System Check

1. **Check GCoMo Power Levels**
 2. Phasecheck
 3. Check PPS Synchronization
 4. Check Time Synchronization
- Use **dbbcifa**, **dbbcifb**, ... commands to check if each used GCoMo has the correct power levels:
 - **dbbcifa/2,20,agc,31433,32000**
 - GCoMo Input (1-Direct Input, 2-Down Conversion)
 - Attenuation level (ideally between 10-40)
 - Automatic Gain Control (agc – AGC on, man – AGC off)
 - Power Level (should close to power target)
 - Power Target (32000 ideal for 4 GHz Input)

Post-Startup System Check

1. Check GCoMo Power Levels
2. **Phasecheck**
3. Check PPS Synchronization
4. Check Time Synchronization

- **Command: checkphase**

- This command will check if phases for the used samplers are correctly aligned
- If the check fails, make sure that the **GCoMo Power Levels** for the failed Board are correct, and repeat the check.
- If the check still fails, **restart the Control Software**. Loading the Firmware can be skipped.
- If the check still fails, there may be a **hardware issue**. Contact Support. Include the latest logfile (in Folder C:\)

Post-Startup System Check

1. Check GCoMo Power Levels
2. Phasecheck
- 3. Check PPS Synchronization**
4. Check Time Synchronization

- **Command: pps_delay**

- Checks the delay between internal (generated) and external PPS
- Should be **below 100ns** for each used IF.
- **Restart Control Software** if Value too high. Loading Firmware can be skipped.
- **Careful:** If the external PPS comes from the GPS, there may be a drift over time between internal and external PPS.

Post-Startup System Check

1. Check GCoMo Power Levels
2. Phasecheck
3. Check PPS Synchronization
4. **Check Time Synchronization**

- **Command: time**

- Check that the **vdif-timestamps** are correct. All timestamps should be identical.
- If not, **check GPS connection** and **restart Control Software**. Loading Firmware can be skipped.

Calibration

Calibration

- When do you need to recalibrate?
 - **Gain:** Core3H-Power is systematically off
 - **Offset:** Core3H-Bstat is systematically off
 - **Delay:** Always recalibrate if you needed to recalibrate gain or offset.
 - Check for **RFI** in the band first, this can in some cases lead to deviation in gain and offset.
- **Only perform calibration if you have a clean 4GHz Signal source:**
 - 4 GHz bandwidth clean noise (from noise generator or receiver)
 - Power must be stable during the calibration process!!!
 - Enough Power (32k GCoMo Power Level)
 - No RFI in the band!!!

Offset-Calibration

1. **Increase the attenuation** of the corresponding GCoMo so that the **power level is between 5 and 10k**:
 - dbbcifa=2,40
 - dbbcifa/ 2,40,man,1,5557,32000;
2. Issue the Command: **cal_offset=board_nr[1-8]**
 - Example: cal_offset=1
 - The result is shown in the Command windows of the Control Software, not the Client:
Sampler[0], best offset 136
offset=1,0,136
Sampler[1], best offset 124
offset=1,1,124
Sampler[2], best offset 120
offset=1,2,120
Sampler[3], best offset 102
offset=1,3,102
3. Change the values in the **config_adb3l.txt** according to the result of the calibration
 - offset=1,0,136
offset=1,1,124
offset=1,2,120
offset=1,3,102
4. **Reset the attenuation** in the GCoMo to agc to reach power level of 32k, restarting the control software is not necessary
 - dbbcifa=2,agc

Gain-Calibration

1. Make sure the power level of the GCoMo is **around 32k**, **manual mode** is recommended:
 - dbbcifa=2,man
 - dbbcifa/ 2,4,man,1,**32443**,32000;
2. Issue the Command: **cal_gain=board_nr[1-8]**
 - Example: cal_gain=1
 - The result is shown in the Command windows of the Control Software, not the Client:
Sampler[0], best gain 129
Sampler[1], best gain 97
Sampler[2], best gain 128
Sampler[3], best gain 159
3. Change the values in the **config_adb3l.txt** according to the result of the calibration
 - gain=1,0,129
gain=1,1,97
gain=1,2,128
gain=1,3,159
4. **Reset the attenuation** in the GCoMo to agc, restarting the control software is not necessary.
 - dbbcifa=2,agc

Delay-Calibration

1. Make sure the power level of the GCoMo is **around 32k, manual mode** is recommended:

- dbbcifa=2,man
- dbbcifa/ 2,4,man,1,**32443**,32000;

2. Issue the Command: **cal_delay=board_nr[1-8]**

- Example: cal_delay=1
- The result is shown in the Command windows of the Control Software, not the Client
0->1, Best difference = 194 with corr_value = 254646768
1->2, Best difference = 142 with corr_value = 254000252
2->3, Best difference = 214 with corr_value = 253237046
Sampler[0]->delay=247
delay=1,0,247
Sampler[1]->delay=441
delay=1,1,441
Sampler[2]->delay=583
delay=1,2,583
Sampler[3]->delay=797
delay=1,3,797

3. Change the values in the **config_adb3l.txt** according to the result of the calibration

- delay=1,0,247
delay=1,1,441
delay=1,2,583
delay=1,3,797

4. **Reset the attenuation** in the GCoMo to agc, restarting the control software is not necessary.

- dbbcifa=2,agc

Links and further information

- The packages with Firmware and Software can be downloaded via the HAT-Lab website: <https://www.hat-lab.cloud/> (registration required)
 - Documentation can be found in the manuals folder of each package
- Python Toolkit for Monitoring and Remote Control can be found under: <https://github.com/mpifr-vlbi/dbbc3>
- A DBBC3-FAQ with further information can be found under: https://deki.mpifr-bonn.mpg.de/Cooperations/DBBC3/DBBC3_FAQ

Contact information

- Commercial aspects:
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- General and Firmware:
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- Hardware:
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Thank you, any questions?