Progress towards commodity signal processing for next-gen DBEs

- A digital backend based on the ROACH2 is being developed at MIT Haystack Observatory that extends the performance and cost advantages of digital processing using commercially available hardware from the CASPER collaboration.

- Builds on code base from Event Horizon Telescope R2DBE

- The ROACH2 DBE improves on the ROACH1 DBE by processing two inputs of 2048 MHz bandwidth, compared to 512 MHz previously. The design uses both VHDL and CASPER blocks to maximize performance and reduce design time. The CASPER filterbanks channelize the input signals which are then re-quantized to two bits and the data are output in VDIF protocol through the 10 GigE outputs.

- Test vectors are used in both hardware and simulation to verify the correctness of the signal processing.

1 R2DBE: A Wideband Digital Backend for the Event Horizon Telescope
Harvard-Smithsonian Center for Astrophysics, Cambridge, MA 02138.
http://iopscience.iop.org/article/10.1086/684513
RDBE-H

- ROACH 1, PFBG-1.4 personality, 32 MHz channels
- NRAO chassis, synthesizer, ALC, DDC personality
- 2IF x 512 MHz iADC (2 Gbps)
- VHDL filterbank
- VSI-S command server
- 3U chassis

ROACH 1 (Reconfigurable Open Architecture Computing Hardware)

- Virtex-5 SX95T
- 640 DSP48E
- Z-DOK+
- CX4 10-GigE
- PPC Linux
- C-code VSI-S server

https://casper.berkeley.edu/wiki/ROACH
PFBG 1.4

- VHDL modules using CASPER code for iADC, 10 GigE
- Complex to Real conversion for Mk5b data format

Number of Slice Registers: 39,303 out of 58,880 66%
Number of Slice LUTs: 33,852 out of 58,880 57%
Number of BlockRAM/FIFO: 82 out of 244 33%
Number of DSP48Es: 296 out of 640 46%
RDBE-G

- ROACH 1, PFBG-3.0 personality, 32 MHz channels
- 2IF x 512 MHz iADC (channel select 2, 4 Gbps)
- GPIO card with off the shelf attenuators
- LCD time, status
- Haystack synthesizer
- Updated server
- Extended Multicast
- PCAL, TSYS
- 2U chassis
RDBE-G

- Designed in Protocase
- 2U chassis height
**PFBG 3.0**

- Parallelized Xilinx cores for FIR / FFT
- CPU thresholds for quantizer
- VDIF packets with complex data (no real conversion)

![Diagram of PFBG 3.0 system](image)

Number of Slice Registers: 30,264 out of 58,880 51%
Number of Slice LUTs: 32,775 out of 58,880 55%
Number of BlockRAM/FIFO: 96 out of 244 39%
Number of DSP48Es: 178 out of 640 27%
ROACH 2 DBE

- ROACH 2, PFBG-4.0 personality, 32 MHz channels
- 2IF x 2048 MHz, ASIAA 5Gsps ADC (2, 4, 8, 16 Gbps)
- GPIO card with off the shelf attenuators
- LCD time, status
- Haystack synthesizer
- Updated server
- Extended Multicast
- PCAL, TSYS
- 1U chassis

(EHT R2DBE, RDBE-G2, RDBE-J, DBE4?)
ROACH 2

- Virtex-6 SX475T
- 2016 DSP48E1
- Z-DOK+
- SFP+ 10-GigE
- PPC Linux
- Python KATCP
- C-code VSI-S server

Number of Slice Registers: 158,319 out of 595,200 26%
Number of Slice LUTs: 110,318 out of 297,600 37%
Number of RAMB36E1/FIFO36E1s: 234 out of 1,064 21%
Number of RAMB18E1/FIFO18E1s: 646 out of 2,128 30%
Number of DSP48E1s: 934 out of 2,016 46%
PFB Blackbox

- CASPER pfb_fir_real, fft_wideband_real, 7 stages
- $2^6$ channels x 32 MHz = 2048 MHz
- Faster XSG compile
- Export .ngc file
- Or export VHDL
- Allows fast simulation

```
c = pfb_coeff_gen_calc(7, 8, 'hamming', 3, 0, 1, -1, false); c = c / (sum(c));
for n = 0:16;
    [resp(n+1,:), f] = freqz(c .* exp(j * n * 2 * pi / 128 * (0:length(c)-1)), 1, 8192, 4096);
end;
plot(f,20*log10(abs(resp')));
xlabel('MHz'); ylabel('dB'); set(gca,'xtick',[0:32:2048]); grid on
```
Simcheck

- Matlab PFB S-Function operates on 8-bit data synced to frame
- Delay output and compare to simulation of PFB

```matlab
if block.OutputPort(1).IsSampleHit
    block.Dwork(4).Data = block.Dwork(1).Data .* block.Dwork(3).Data;
    block.Dwork(5).Data = sum(reshape(block.Dwork(4).Data,128,8),2); %fir sum across rows
    block.Dwork(6).Data = fft(block.Dwork(5).Data);
    block.OutputPort(1).Data = block.Dwork(5).Data*32;
    block.OutputPort(2).Data = real(block.Dwork(6).Data(1:64)/1024);
    block.OutputPort(3).Data = imag(block.Dwork(6).Data(1:64)/1024);
end
```
PFB simulation results

- Swept sinusoid processed by Matlab function
- Output of PFB Blackbox
- Error $\sim 1e-5$ ($\sim 2^{-16}$)
VHDL check

• Compare Simulink to VHDL output

• Identical result
PFBG 4.0

- 2IF x 2048 MHz bandwidth
- Test Vector Generator $2^{16}$ points
- $\text{tvg} \rightarrow \text{pfb} \rightarrow \text{quant} \rightarrow \text{chsel} \rightarrow \text{simcheck}$
- Channel select 2, 4, 8 Gbps per IF
- Phase Cal extraction
- Total Power 80Hz
simcheck

- Checks PFB, quantizer and channel selector
MAP, PAR, Planahead reports

- XSG->XST resynth->EDK->Planahead UCF->EDK MAP PAR...

- MAP, PAR options in fast_runtime.opt

  Command Line : map -equivalent_register_removal off -lc off -timing
  -detail -ol high -xe n -mt 2 -register_duplication
  on -o system_map.ncd -w -pr b system.ngd system.pcf

  Target Device : xc6vsx475t
  Target Package : ff1759
  Target Speed : -1
  Mapper Version : virtex6 -- $Revision: 1.55$
  Mapped Date : Tue Oct 11 07:32:39 2016

Design Summary
-------------
Slice Logic Utilization:
- Number of Slice Registers: 158,319 out of 595,200 26%
- Number of Slice LUTs: 110,318 out of 297,600 37%

Specific Feature Utilization:
- Number of RAMB36E1/FIFO36E1s: 234 out of 1,064 21%
- Number of RAMB18E1/FIFO18E1s: 646 out of 2,128 30%
- Number of DSP48E1s: 934 out of 2,016 46%

Total REAL time to MAP completion: 37 mins 46 secs
Total CPU time to MAP completion (all processors): 38 mins 40 secs

ruu-smc-xilinx:~ Tue Oct 11 08:10:34 2016
par -xe n -w -ol high -mt 4 system_map.ncd system.ncd system.pcf
  Number of Slice Registers: 158,319 out of 595,200 26%
  Number of Slice LUTs: 110,318 out of 297,600 37%
  Number of RAMB36E1/FIFO36E1s: 234 out of 1,064 21%
  Number of RAMB18E1/FIFO18E1s: 646 out of 2,128 30%
  Number of DSP48E1s: 934 out of 2,016 46%

Total REAL time to PAR completion: 14 mins 6 secs
Total CPU time to PAR completion (all processors): 22 mins 11 secs
Xilinx Planahead

- Assign pbblocks based on Simulink modules, netlist primitives
- Constrain DSP48, BRAM or logic slice
- Overlap allows sharing of unused elements
- Assigning logic slices increases routing for CASPER software registers OPB bus
- Channel select unconstrained. VDIF, tgbe loosely constrained
- Aim for ~60% utilization DSP, BRAM including overlapped area
Logic Layout

- Logic colored according to pblock
- Slices extend beyond pblock boundaries
- Unconstrained logic around pblock boundaries and central areas
Logic Layout

- DSP logic elements extend far from DSP and BRAM pbloc
Routing congestion, LUT utilization
10 GbE capture

- Python program FPGA
- Program TVG
- Set thresholds
- Channel sel
- Tcpdump

```python
# program fpga
roach2.progdev('dbe4_2016_Sep_28_1940_reorder_chsel.bof')
# calibrate ADCs
# arm the one pps
# write tvg
roach2.write_int('tvg0_tvg_sel', 1)

t = np.arange(2**12*16)
tvg = t*0.0
for ch in range(16):
    tvg += np.sin(2*np.pi*(ch*32+ch/16.0)*1e6*t/4096e6)
tvg *= 64/max(tvg)
plt.figure(); plt.plot(tvg); plt.show(block=False)
for ram in range(16):
    roach2.write('tvg0_tvg_adc_' + str(ram), struct.pack('>4096b', *tvg[ram::16]))

# set thresholds
thresh=800
for q in range(8):
    for ch in range(8):
        roach2.write_int('quant0_quant' + str(q) + '_quant_ram', thresh ,0 , ch)

# chsel
for reg in range(64):
    chs=((reg*4+3)<<24)+((reg*4+2)<<16)+((reg*4+1)<<8)+(reg*4)+0
    roach2.write_int('chsel0_registers_sel' + str(reg), chs)

# program 10GbE
# program VDIF
```
Success!

```
sudo tcpdump -i eth2 src 192.168.10.11 -s 0 -c 1000 -w /tmp/junk.pcap

[invalid, legacy, sec, unass, refepoch, frame, ver, chns, len, cplx, bits, thread, station, edv, euda, eudb, psn, sync, dat, bstater, bstatei]= rd_vdif('/tmp/junk.pcap', 1:100, 0:15, 1);
figure;for ch = 1:4;subplot(4,1,ch);hold on;plot(real(dat(ch+1,1:512)),'r');plot(imag(dat(ch+1,1:512)),'b');title(["Channel ", num2str(ch)]);end;xlabel("Sample");
```
SKARAB

- Virtex-7 VX690T
- 4 x 40 GbE QSFP+
- Hybrid Memory Cube